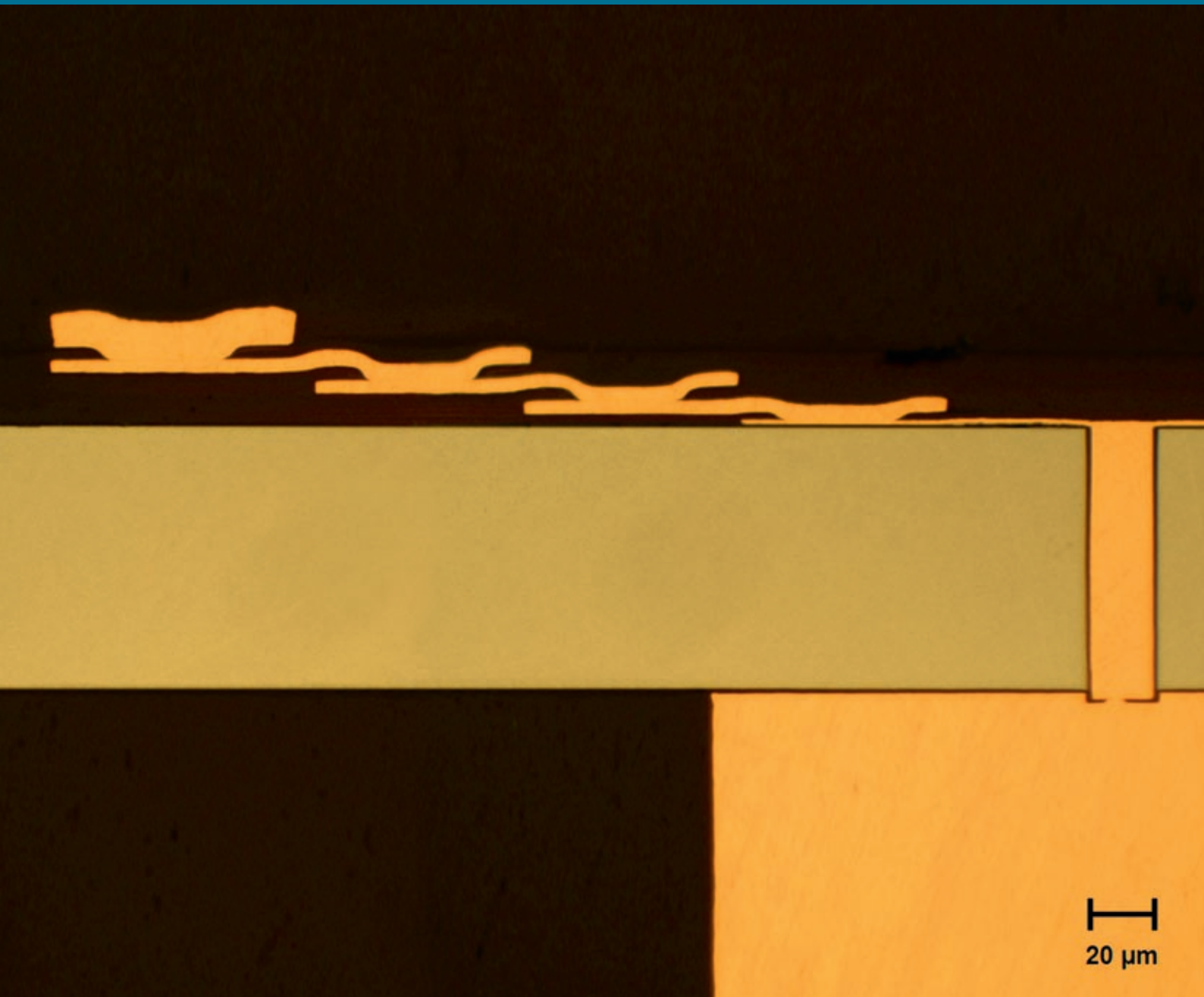


**DEPARTMENT OF
HIGH DENSITY INTERCONNECT &
WAFER LEVEL PACKAGING**



HIGH DENSITY INTERCONNECT & WAFER LEVEL PACKAGING

ELECTRONIC PACKAGING AT FRAUNHOFER IZM

The Fraunhofer Institute for Reliability and Microintegration IZM is one of 59 Fraunhofer Institutes conducting applied research predominantly in the realm of science and engineering. Fraunhofer IZM's services from the realm of electronic packaging and smart system integration are solicited by customers and contractual partners in industry, the service sector and public administration.

Electronic packaging is at the heart of every electronic application; it interconnects the individual components, protects the electronic systems against vibration and moisture and dissipates heat reliably. In short, it ensures that electronics continue to function reliably in even the harshest conditions. Clever packaging also reduces the manufacturing costs for complex electronic systems. With its application-oriented research Fraunhofer IZM bridges the gap between microelectronic component providers and technical system manufacturers in a broad range of industries, such as automotive or medical technologies. Since its foundation in 1993 Fraunhofer IZM has enjoyed an extremely successful cooperation with TU Berlin's key research area Technologies of Microperipherals and currently has four branches in Berlin, Dresden and Oberpfaffenhofen, with 180 full-time employees and 136 PhD candidates, apprentices and diplom students.

HIGH DENSITY INTERCONNECT & WAFER LEVEL PACKAGING

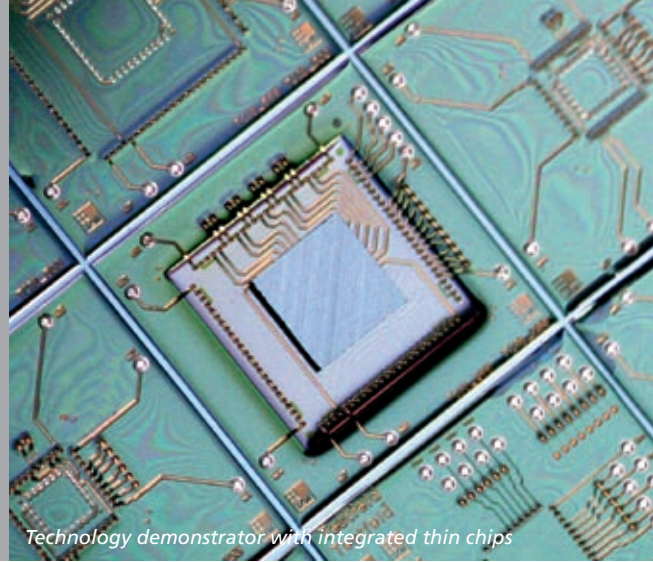
The department High Density Interconnect & Wafer Level Packaging focuses on the development and application of thin-film processes in microelectronic packaging. Production-compatible equipment for thin-film processing in an 800 m² clean room determines the technological possibilities. The department cooperates with manufacturers and users of microelectronic products, as well as with clean room equipment producers and material developers from the chemical industry from all over the world.

The well-established technology branches offer prototyping and small-volume production as a regular service within the realms of MCM-D, wafer-level CSP with redistribution routing, 3D integration and wafer-level bumping for flip chip mounting to both industrial partners and customers.

Processable wafer size is limited from 100 mm to 200 mm. Together with our Dresden site the processing of 300 mm wafers is also possible. The service in the above areas can also include a technology transfer even to customer-specific tools. In numerous R&D projects, ongoing skills and know-how are being developed, which can be passed to SME-partners on a development stage.

CORE COMPETENCIES

- **3D integration**
Interposer, through Silicon vias (TSV), thin chip integration, 3D packaging of image sensors, redistribution to the backside of the wafer, thin wafer handling
- **Wafer-level CSP**
Cu redistribution, polymer dielectrics, package singulation, reliability investigation
- **Wafer bumping**
Electroplating of structures in photo resist masks, copper pillars, micro bumping for pixel detectors; optical inspection
Bumping materials Cu, Ni, Au; SnAg, AuSn, SnPb, Sn, In;
- **Thin film multilayer**
Customer-specific layout, multilayer routing, integrated passives, chip-first, flip chip
- **Micro energy systems**
Wafer-level battery, micro fuel cell, hermetic sealing



3D INTEGRATION BY THROUGH SILICON VIA TECHNOLOGY (TSV)

High Density Interconnect and Wafer Level Packaging develops TSV technologies to enable heterogeneous 3D integration of multiple devices such as sensors, processors, memories and transceivers with excellent electrical performance and small form factor. All developments are done with special focus on industrialization and process integration. Based on that, close co-operations with equipment and material suppliers are formed to allow prototyping and small volume production of customized 3D systems for industrial applications like automotive, medical and communication.

In this context especially silicon interposers with through silicon vias have become key components of 3D architectures. Due to the combination of high density TSVs and multi layer wiring silicon interposers allow to adapt fine pitch IOs from components mounted on their top side to more relaxed IO geometries on their bottom side. The use of electroplated copper as conductive material and low loss polymer as interlayer dielectric material enables high performance signal transmission without serious losses by parasitic effects.

Basic technologies for the silicon interposer fabrication are dry etching of silicon, isolation and filling of the silicon holes, multi layer wiring based on electro plated copper and polymer dielectric as well as thin wafer backside processing based on wafer thinning and thin wafer handling by temporary wafer bonding and de-bonding.

3D INTEGRATION BY THIN CHIP INTEGRATION

Heterogeneous integration bridges the gap between micro-electronics and its derived applications. Currently MEMS and the associated signal processing ASICs are produced and packaged at different industry sectors (different fabs). To reduce cost and at the same time enhance yield and performance this quite expensive way of packaging has to be overcome. A different packaging concept has been developed at Fraunhofer IZM. It uses standard redistribution layer technology to mount thinned chips on a full wafer substrate e.g. thinned ASIC chips on a MEMS wafer. For this approach no through silicon vias are needed. Standard chips can be used without redesign. Only known good dies are packaged with the cost benefit of wafer-level technology.

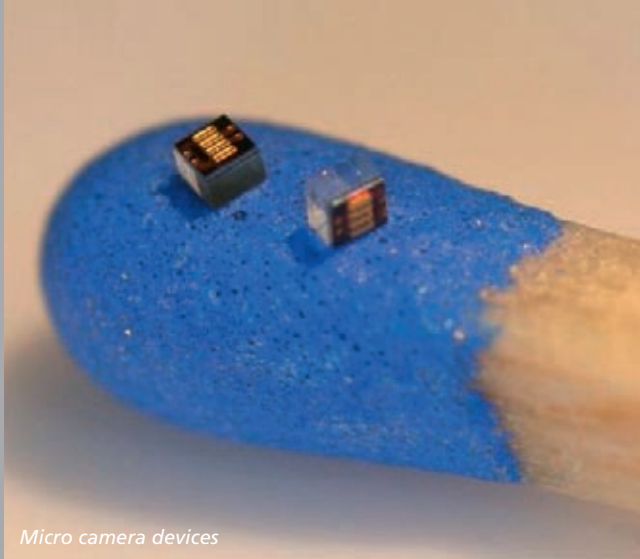
The process flow is: The larger chip (on wafer level) works as carrier. The smaller chips are thinned down to a thickness of typically 10–30 μm. Then they are glued (on chip level) face up onto the larger chips of the carrier wafer. Both chips are then connected with a standard RDL and finally balled and singulated. This technology has been demonstrated in different projects:

Project "E-cubes":

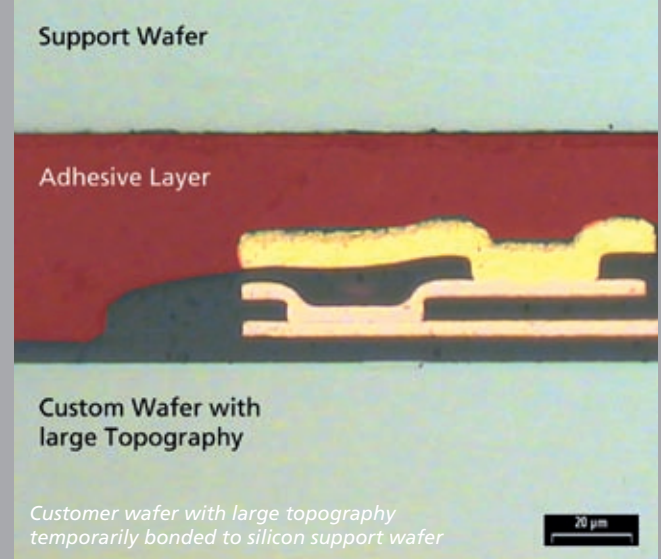
Realization of highly miniaturized, truly autonomous systems for ambient intelligence.

Project "Restles":

Chip scale package integration of different micro system technologies (MEMS and ASIC) for automotive applications.



Micro camera devices



Customer wafer with large topography temporarily bonded to silicon support wafer

3D INTEGRATION FOR MICRO CAMERA DEVICES

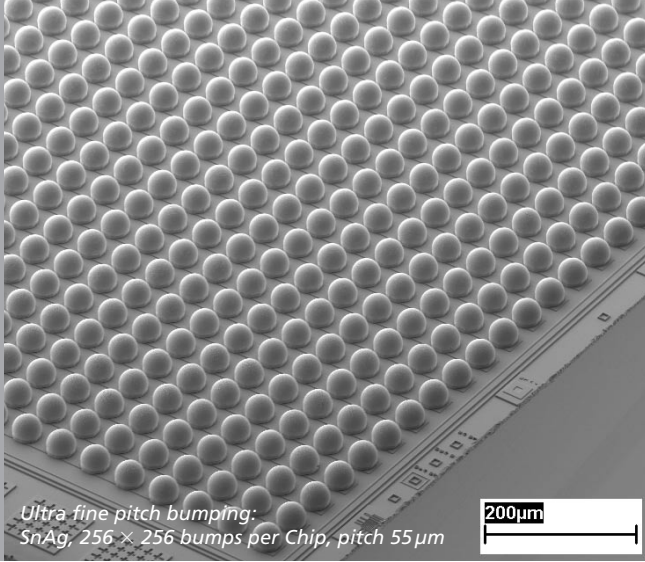
The ongoing efforts to miniaturize the pixel sizes of CMOS imagers enabled the fabrication of camera devices with very small dimensions and comparably high resolutions. Such micro cameras are often significantly smaller than $1\text{ mm} \times 1\text{ mm}$ and favourably needed in medical applications such as endoscopes. In the automotive industry there is research in what extent such cameras can be applied as novel input device or in driver assistance systems. If the rearview mirrors are replaced by micro cameras the flow resistance is reduced significantly, which contributes to an enhanced energy efficiency of the vehicle.

To benefit from the small size of the image sensors it is necessary to integrate the optics while keeping the form factor of the package small. At Fraunhofer IZM a process chain was developed, allowing the fabrication of micro camera devices, which is completely carried out at wafer-level. The CMOS wafer is bonded onto a glass wafer and thinned down. After contacting the chip using through silicon vias, the redistribution layers are applied as well as the bumps. The integration of the optics and image sensors is done in the last process step by wafer bonding before the devices are singulated, which saves a cost-intensive assembly of individual optics. This technology allows the production of micro camera devices with a volume of well below 1 mm^3 .

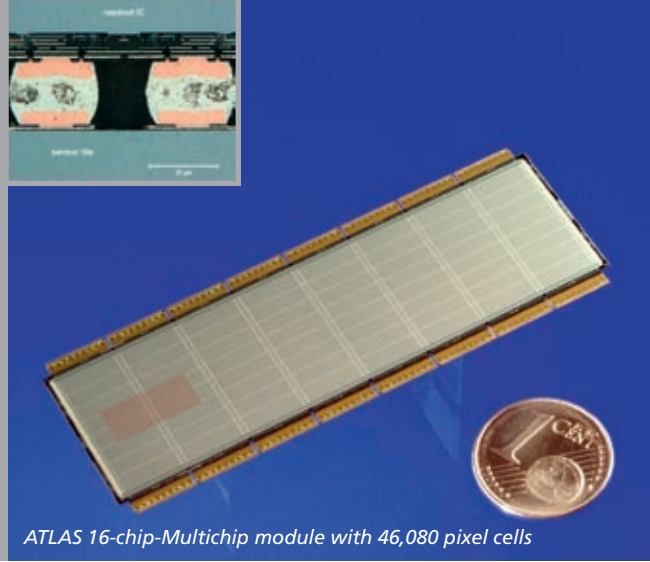
PERMANENT AND TEMPORARY WAFER TO WAFER BONDING

For permanent bonding application such as wafer level MEMS and opto packaging different materials and bond processes are available. Adhesive bonding can be performed by using transparent or non transparent glue materials, which can be cured by UV exposure or heat. The glues can be applied by spin coating to gain a continuous bond layer or by glue transfer, which allows coating only topography features with glue and leaving the remaining structures non-coated. Further available permanent bonding methods are wafer to wafer soldering based on pre-deposited metal structures like Au+Sn or Cu+Sn or anodic bonding of silicon and alkaline content glass material. Prior to all bond processes the wafers can be positioned to each other by face to face or back to face alignment with an accuracy $> 5\text{ }\mu\text{m}$.

Furthermore different temporary wafer bonding and de-bonding technologies are available, which allow bonding customer wafers temporarily to carrier wafers and removing them after the backside processing of the customer wafers is finished. Due to the special design of carrier wafer, adhesive and de-bonding equipment different release mechanisms are available to finally de-bond both wafers from each other. Basic methods are solvent release without heat, slide-off release at elevated temperatures and laser release using a transparent carrier. Based on the configuration of the customer wafer (topography, thickness, kind of processes to be applied) as well as the subsequent second level assembly of the components, the most suitable handling concept and wafer support system can be chosen.



Ultra-fine pitch bumping:
SnAg, 256 × 256 bumps per Chip, pitch 55 μm



ATLAS 16-chip-Multichip module with 46,080 pixel cells

WAFER BUMPING BY ELECTROPLATING

Wafer bumping by electroplating has the largest potential for realizing highest I/O densities with a pitch range from 200 μm to 20 μm at a high quality standard.

The fabrication sequence can be divided into basic process steps, which are sputtering of the UBM, lithographical printing of the photo resist pattern, electroplating of microstructures, differential etching of the plating base, and if required a final solder reflow.

The electroplating technique accommodates a variety of metals and metal alloys to support the demands of a great number of applications. With the plating line installed at Fraunhofer IZM, solder bumps consisting of SnPb63, PbSn5, SnAg3.5, SnCu0.7, AuSn20, and pure Sn can be generated as well as straight-wall bumps like Cu/Sn, Ni/Au, and pure Au. Different photo resist systems with a large variety of layer thicknesses enable the deposition of flat pad metallization as well as high pillar bumps up to 120 μm with high depth-to-width aspect ratio and steep slopes. Especially for flip-chip bonding of thermal sensitive devices, an Indium bumping technology using electroplating has been developed at Fraunhofer IZM. Furthermore, the fabrication of nano-porous Au bumps on wafer level can be done for low-temperature TC bonding.

All kinds of semiconductors such as silicon, SiGe, GaAs, and InP as well as ceramic and quartz substrates can be processed by wafer bumping using electroplating.

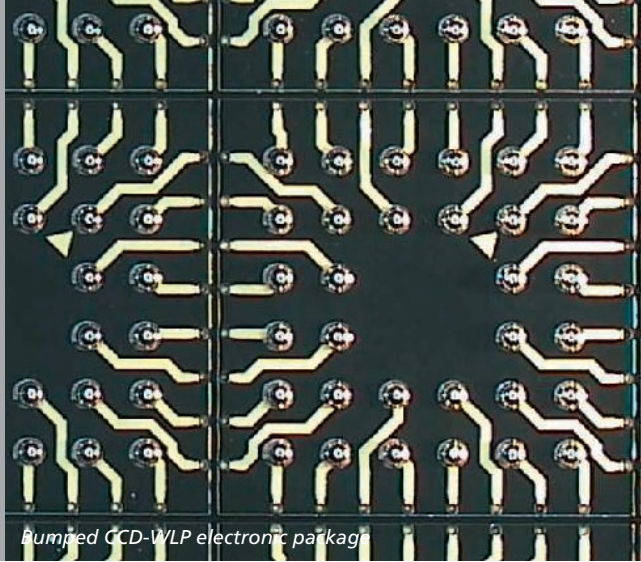
The bumping technique at Fraunhofer IZM is well established on 100mm through 200mm wafers, and will shortly be qualified for 300mm wafers. Prototyping as well as volume production of bumped wafers can be offered as a service.

WAFER BUMPING FOR PIXEL DETECTOR APPLICATIONS

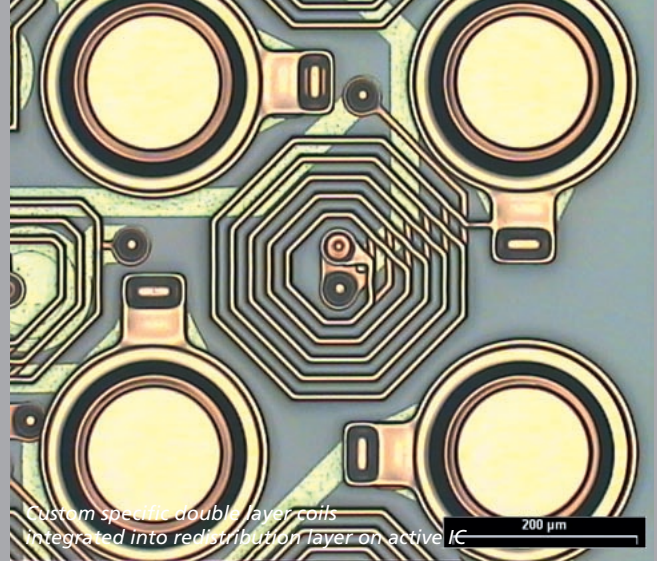
Hybrid pixel detector modules are now state-of-the-art in high energy particle detection. These modules consist of a particle sensing element, the sensor, and one or more electronic readout chips which are flip-chip bonded to the sensor tile.

One advantage of hybrid pixel detectors is the separate development, optimization and processing on wafer level of sensor and electronic readout chip. Because of the direct interconnection between pixel and readout cell the high spatial resolution demands small solder joints in a tight pitch for an accurate and fast detection of the particle track location. ECD-bumping (electrochemical deposition) is therefore the best suited technology because it can be used for pitches even below 40 μm. 25 μm pixel interconnection bumps are produced by SnPb, SnAg or AuSn electroplating on 200 mm readout chip wafers with an excellent uniformity. Solderable metallization has to be deposited on the sensor pixel pads. Sensor chips of different materials can be processed ranging from silicon and GaAs wafer to single chip diamond substrates.

Fraunhofer IZM has long term experience in manufacturing of hybrid pixel detector modules from research and development stage up to the production of more than 1000 modules for large particle detector projects. Pixel detector modules manufactured at Fraunhofer IZM are the innermost part of two of the largest particle detectors world-wide, the ATLAS and CMS detector at the Large Hadron Collider (LHC) at CERN, Switzerland.



Bumped CCD-WLP electronic package



Custom specific double-layer coils integrated into redistribution layer on active IC

WAFER LEVEL REDISTRIBUTION TECHNOLOGY

Polymers play a major role in the built-up structure of redistribution (RDL). The dielectric layer is one of the key layers which could act as a stress buffer between IC and PWB. Low K materials are preferred because a high capacitance reduces the computing speed between integrated circuits. In addition, the selection of the optimal polymer for a given application depends not only on its physical and chemical properties and processability, but also on its intrinsic interfacial characteristics. Several different redistribution processes have been developed, but main process steps are similar to each other. Differences exist mainly in the material selection.

First a dielectric layer is deposited on the wafer to enhance the passivation layer of the die. Using photosensitive polymers requires fewer processing steps for thin film wiring than non-photosensitive materials that have to be dry etched. Fraunhofer IZM uses BCB, PI, PBO or Epoxy depending on the application. The rewiring metallization consists of electroplated copper traces to achieve a low electrical resistivity. A sputtered layer of Ti:W-Cu (200/300 nm) serves as a diffusion barrier to Al and as a plating base. A second polymer layer is deposited to protect the copper and to serve as a solder mask. Electroplated Ni/Au is used for the final metallization. Solder balls are deposited by solder printing or ball-drop directly on the redistributed wafers.

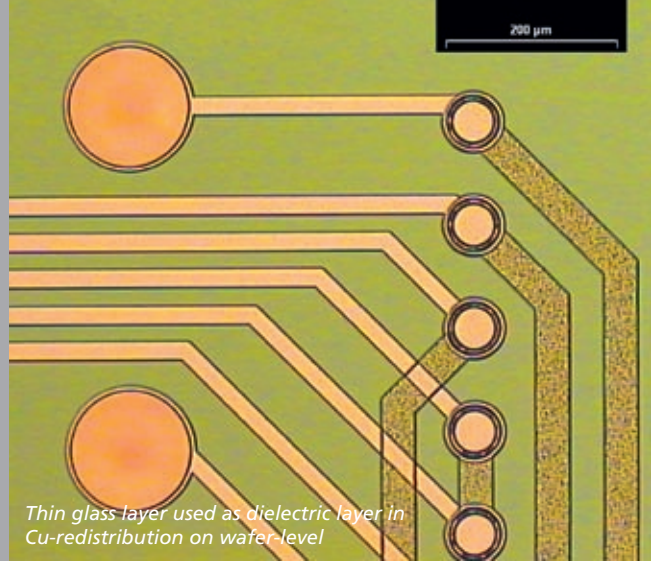
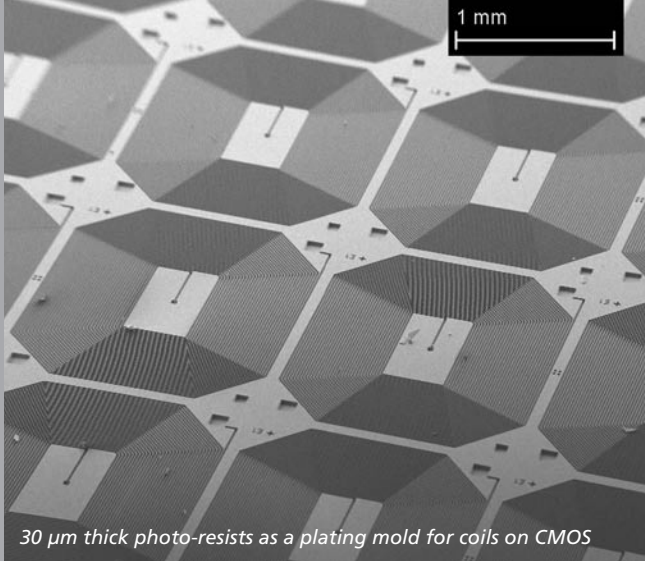
THIN FILM INTEGRATION OF PASSIVE COMPONENTS

All three kinds of passive components (L, R, C) can be integrated into thin-film multilayer wiring and redistribution layers on different types of substrate wafers.

Single and double layer inductors are realized by using at least two metal layers, that are separated by one polymer dielectric layer. Depending on the electrical requirements square, round, octagonal or arbitrary winding shapes can be done with line widths and spaces down to $4\mu\text{m}$ and height to width aspect ratios larger than 1. By using electroplated copper as conductive and low loss polymers as inter dielectric layers, high quality factors can be obtained.

The same layer construction is used to fabricate small value metal-insulator-metal capacitors suitable for RF and timing applications. Due to the low dielectric constant of the polymer dielectric the capacitance density is in the range of some pF/mm^2 . In order to obtain higher capacitance densities, the regular polymer is replaced by other Para dielectrics such as thin glass layers or tantalum oxide. In this case capacitance densities up to several nF/mm^2 are possible.

For thin film resistor integration sputtered Nickel/Chromium (NiCr) with a sheet resistance of $100\text{Ohm}/\text{square}$ is used. The NiCr is structured by negative technology using wet etching to create resistor meanders with minimum line width of $10\mu\text{m}$. Thus total resistance values between 100Ohms and several hundred kOhms can be fabricated.



THIN FILM POLYMERS AND PHOTO-RESISTS

Polymers are a key building block for all WLP and related technologies like IPD (integrated passives devices) and 3D-SiP (system in package). A couple of different classes of photo-sensitive polymeric materials are available for integration at Fraunhofer IZM: Polyimide (PI), Polybenzoxazole (PBO), Benzocyclobuten (BCB), Silicones, Acrylates and Epoxy. Depending on your application we will find the best combination. For example curing and the resulting shrinkage play an important role due to temperature sensitive devices and the topography of the metallization to be passivated. Test structures are available for a wide range of mechanical and electrical properties. The mechanical properties have a strong influence on the reliability of non-underfilled WLP. There can be different failure modes using different polymers for WLP on FR4 boards.

Photo resists are photo-sensitive polymer-based materials that are applied temporarily on the wafer mostly for plating or etching. The base resin of positive-tone photo resists is typically Novolak whereas negative-tone resists are based on acrylate or an epoxy resin. Negative dry film resist is developed mostly with environmentally friendly aqueous carbonate developer. Fraunhofer IZM offers a broad spectrum of different kinds of photo-resists together with spin-coating, spray-coating or lamination.

THIN FILM GLASS DEPOSITION *

Borosilicate glass is well known for its outstanding physical, chemical, optical and biomedical properties. Its robustness, chemical durability as well as its temperature and long-term stability makes it an ideal material for electronic packaging and surface passivation.

Lithoglas™ enables the use of borosilicate glass as hermetic and robust thin-film for a large variety of different substrates and applications including power semiconductor, optical devices, automotive as well as consumer products.

The unique deposition process allows for low substrate temperatures during processing. Though being fabricated at about 80°C, the glass thin-films yield temperature stable (TG ≥ 530°C) hermetic coatings. Good adhesion and excellent reliability is proven on many substrates including semiconductors, metals and polymers. Thermal expansion is perfectly matched to silicon.

Microstructuring of the borosilicate thin-film is feasible using lift-off lithography down to 1.5 μm lines and space. This additive method protects uncoated areas by photo resist during deposition.

The processes and products are compatible with CMOS-backend processing and comply with today's industrial and environmental regulations.

* In Cooperation with MSG Lithoglas AG



Clean room



Spray coating of resist

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