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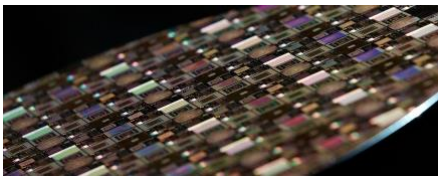

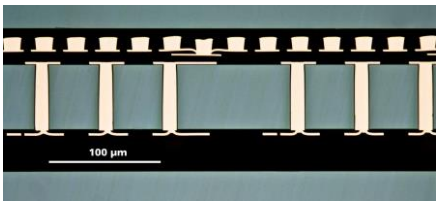

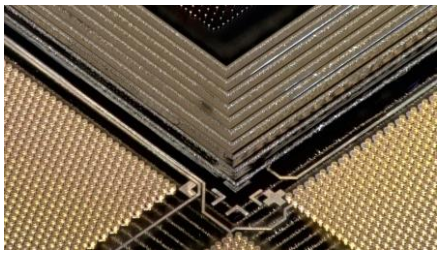

3D SYSTEM INTEGRATION TSV INTERPOSER

Silicon interposers with Through Silicon Vias (TSVs) are an important element for 3D system-in-packages (SiP) approaches. Main advantages of silicon interposers are the decoupling of front end and backend processing for the implementation of TSVs, redistribution layers (RDL) and the integration of active and passive devices.
Interposer-based SiPs provide small form factors, excellent electrical properties, heterogeneous device integration, cost effective manufacturing and fast time-to-market.

TSV interposers are specified for various application areas which results also in different technical features ranging from high density TSV integration and high density RDL for digital applications to interposer for RF application as well as MEMS integration and optical interconnects.

Services for 300/200 mm wafers that are offered by Fraunhofer IZM according to industrial specifications include:

- Interposer SiP
- Customer specific design based on defined design guidelines
- Fabrication of high density silicon interposer with TSV and multi-layer redistribution
- Typical interposer features:
  - TSV diameter: 5/10/20 µm
  - TSV depth: > 100 µm
  - Cu-multilayer redistribution layer
- Integration of passive elements
  e.g. R, L, (C)
- Interconnect formation (micro bumps, Cu-Pillar, SnAg)
- Reliability assessment including thermo-mechanical and electrical characterization
- Prototyping, Low-Volume manufacturing

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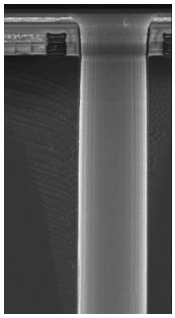

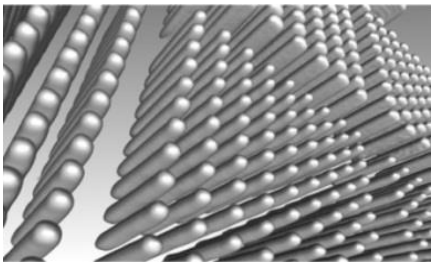

3D TSV INTEGRATION

Through Silicon Vias (TSV) are a key element for 3D wafer-level system integration. Fraunhofer IZM-ASSID has developed a TSV process (POR) for customer-specific applications and supports the evaluation and qualification of new materials for isolation, barrier / seed and TSV filling as well as the optimization of TSV post-processing (front side and back side). All processes are carried out using leading-edge, industry-compatible process equipment for 8" / 12" wafers.

Services for 300 (200) mm wafers that are offered by Fraunhofer IZM-ASSID include:

- Full Cu-TSV integration in active CMOS device wafers
- TSV process integration: via-middle/ via-last TSV, back side via-last
- Dry etch / wet cleaning
- Oxide liner deposition
- Barrier/seed-layer deposition (PVD), MOCVD, Ti, TiN, Ta, Cu
- TSV metallization : Cu-ECD
- Metal anneal up to 400°C
- Front side / back side contact formation
- Basic design guidelines (diameter / depth):
  - min. 5 µm / 50 µm
  - typ. 10 µm / 120 µm
  - 20 µm / 120µm
  - Back side TSV (Cu-liner) up to 250 – 700 µm depth

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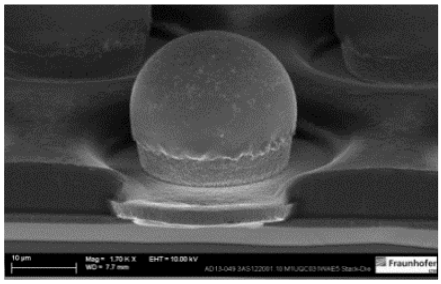

WAFER BUMPING ELECTROCHEMICAL DEPOSITION

IZM provides qualified bumping services in silicon wafers (active/passive).
Micro bump structures of Cu, Cu-SnAg, SnAg, Cu-Ni-Au and Ni-Au are realized by electrochemical deposition with UBM metallization on 300/200 mm wafer. A fluxless reflow is used for solder bump reflow.

Services includes:

- Generation of mask design
- Application of photo polymer as protective layer
- Micro bumping on polymer ILD
- Micro bumping on I/O pad
- Copper bumping on polymer ILD
- Wafer dicing of bumped wafers
- Thinning of bumped wafers
- 2D/ 3D micro bump inspection (AOI) and mapping
- Material- and Equipment Evaluation

µ-Bump Materials

Bump:	Cu / SnAg
	Cu pillar bump
Pad Modification:	Cu / Ni / Au, Cu / Ni, Cu

Standard Design Guide Lines

12" wafer
Customer specific bumping on request

µ-Bump on Polymer

Polymer Via:	15 µm	35 µm
Bump Diameter:	35 µm	55 µm
Bump Pitch:	60 µm	100 µm
Bump Height:	25 µm	30 µm

µ-Bump on Pad

Bump Diameter:	25 µm
Bump Pitch:	min. 55 µm

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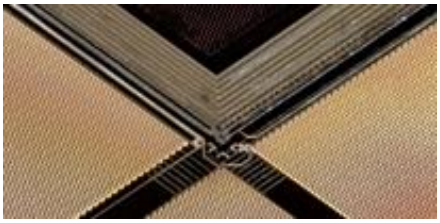

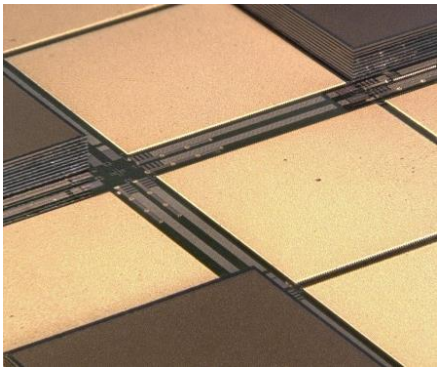

3D ASSEMBLY & STACKING

The following industrial services are offered by Fraunhofer IZM-ASSID:

Plasma Cleaning/Activation

- Micro wave based plasma activation and cleaning
- Process gases: Ar, O_2, forming gas
- Maximum sample size (LxWxH): 300x300x5 mm

Flip Chip Bonding

- Die-to-Wafer (D2W) Bonding
- Flux-activation or fluxless
- Dispensing Pre-applied underfill
- Inline or external reflow
- Die size: 3 – 30 mm
- Die thickness: ≥ 50 µm
- Minimum pitch: ≥ 45 µm
- Min. interconnect diameter: ≥ 25 µm
- Placement accuracy: 3 – 10 µm @3sigma
- Die feed: 300mm Plastic Film Frame Carrier (Disco Type), WafflePack or GelPack (no Flip)

External Reflow

- Belt furnace
- 16" conveyor mesh belt
- 4 pre-heating zones (max. 300°C)
- 1 peak zone (max 400°C)
- 600 mm/ 23,62" cooling section
- Ability to monitor O2/N2 levels 30 ppm
- Gas circulation per heating zone 600 m³/h - 1200 m³/h

Vacuum Reflow

- Single wafer chamber
- Vacuum: 10-2 / 10-3 mbar
- Anneal temperature: ≤ 450 °C
- Temperature uniformity: ± 2 K
- Heating rate: ≥ 20 K/sec
- Cooling rate: ≤ 10 K/sec
- Purging and activation with nitrogen and formic acid
- free programmable gas flow, vacuum, process times and temperatures up to 50 steps

Flip Chip Underfill Dispensing

- Dispensing of various underfill materials
- Total needle placement accuracy: ≥ 50µm @ 3sigma
- Different fluid pump systems (Line DU and Smart Stream)
- Edge Detection Vision Algorithm
- Automatic dispense mass calibration
- Height measurement sensor
- Substrate and needle heating
- Automatic needle cleaning and detection
- Maximum sample size (LxWxH): 300x300x50 resolution, 20 µm

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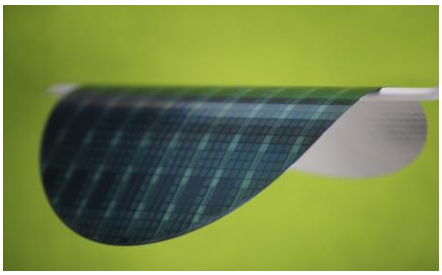

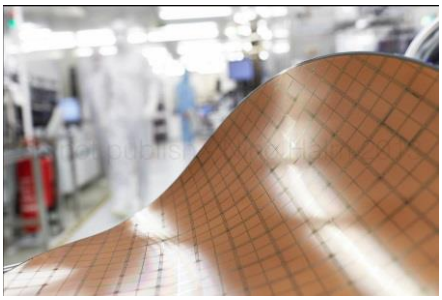

WAFER THINNING

Fraunhofer IZM-ASSID offers services for wafer thinning (8"-12") based on grinding and polishing with and without topography e.g. bumped wafers.

Back Grinding Tape Lamination

- Back Grinding (BG) Tape Lamination of 300 (200) mm UV and Non-UV tapes

Wafer Backgrinding

- Back grinding technologies:
  - Grinding Before Dicing (GBD)
  - Dicing before Grinding (DBG)
  - 300 mm TAIKO Grinding
- Wafer Backgrinding/Polish of 300 (200) mm single wafers
  - Rough grinding: mesh 320, mesh 600
  - Fine grinding: mesh 1500, mesh 4000, mesh 6000
  - Dry polish: Ra 0.0003µm, Ry = 0.0017µm
  - Stress relief etch: SF6 or CF4 based
  - Incoming wafer thickness: ≥ 500µm
  - Outgoing wafer thickness: ≥ 50µm
  - TTV: ≤ 5µm pending on wafer frontside topology
- Wafer Backgrinding/Polish of 300 (200)mm temporary bonded wafer stacks
  - Rough grinding: mesh 320, mesh 600
  - Fine grinding: mesh 1500, mesh 4000, mesh 6000
  - Dry polish: Ra 0.0003µm, Ry = 0.0017µm
  - Stress relief etch: SF6 or CF4 based
  - Incoming wafer thickness: 700 – 1600µm
  - Outgoing device wafer thickness: ≥ 20µm
  - TTV: ≤ 5µm pending on incoming topology of application

Wafer Mounting, Peeling, Exposure

- Inline wafer mounting and BG tape peeling of 300 (200) mm single wafers on 300 (200) mm Film Frame Carrier (Disco type, metal or plastic film frame carrier)
- Application of various UV- and Non-UV dicing tapes including DAF-tape
- Inline exposure of UV-tapes
- Packing and transportation of Film Frame Carrier in 300 (200) mm Film Frame Shipper

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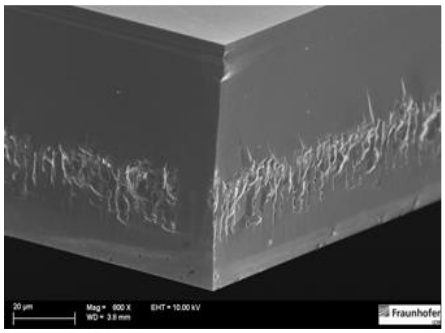

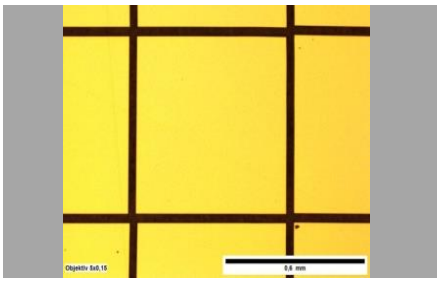

WAFER SINGULATION / DICING

The following industrial services are offered by Fraunhofer IZM-ASSID:

Wafer Singulation - Mechanical Blade Dicing

- Mechanical blade dicing of 300 (200) mm single wafer (50 – 775µm thickness)
- Dicing technologies: Single Cut (Dual Cut), Step Cut, Half Cut (Dual Cut)
  - Grid type: SD
  - Grid size: mesh 1700 – 3500 (pending on blade type)
  - Kerf width: 0,025 – 0,06mm (pending on blade types)
  - Exposure height: 0,38 – 1,24mm (pending on blade type)

Wafer Singulation - Laser Grooving

- Dicing technology: Q-switch pulsed UV-Laser (50 kHz) with wave length of 355nm
  - Spin coating of surface protection film before laser grooving
  - Grooving of lowk materials in dicing street (single grove, dual groove)
  - Laser full cut of ultra thin dies (≥ 50µm)
  - Cleaning wafer surface from protection film

Wafer Singulation - Laser Stealth Dicing

- Dicing technology: High throughput laser engine for silicon singulation (dry process)
  - Applicable to higher doped wafers (> 0,02 Ohm*cm)
  - IR- camera allows wafer recognition also from back side
  - Applicable to ultra-thin wafer, single standard wafer, compound wafer
  - Applicable for sample preparation in physical failure analysis (extremely shorten preparation time in cross-sectioning)
  - Wafer expansion and Remounting

Wafer Edge Trimming

- Grid type: SD
- Grid size: mesh 1700 – 2000 (pending on blade type)
- Kerf width: 0,5 – 1mm (pending on blade types)

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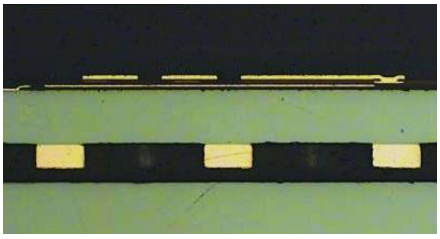

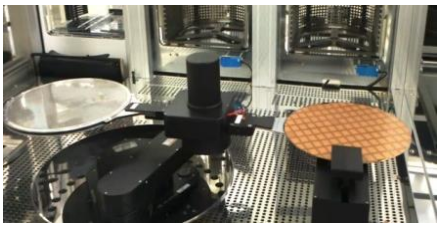

TEMPORARY WAFER BONDING / DEBONDING

Fraunhofer IZM-ASSID offers service for temporary wafer bonding /debonding (8"/12" wafers) and permanent wafer bonding (8"/12" wafers)

Temporary Wafer Bonding

Wafer diameter: 300 (200) mm

- Coating and pre-baking of various wafer bond adhesives
- Bonding forces: 100N up to 60kN (programmable profiles)
- Process vacuum: ≤ $1*10^{-5}$mbar
- Process temperatures: ≤ 550°C with programmable profiles

Wafer De-Bonding

- Wafer diameter: 300 (200)mm
- Slide-off debonding with temperatures up to 350°C
- EdgeZone-Release debonding at room temperature
- Thin wafer handling down to 100 µm thickness
- Wafer flipping capability
- Wafer cleaning after de-bonding with different adhesive solvents
- Wafer mounting on film frame carrier

Permanent Wafer Bonding

- Wafer diameter: 300 mm
- Alignment accuracy: 1.5µm @ 3 sigma
- Flip Chip Bonding (Soldering)
- Bonding under different atmospheres: Air, Formic Acid, N_2
- Bonding forces: 100N up to 60kN (programmable profiles)
- Process temperatures: ≤ 550°C with programmable profiles
- Anodic Wafer Bonding
- High voltage power supply 2000V / 50mA
- Bond current resolution 20µ

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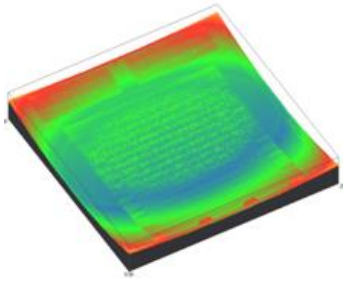

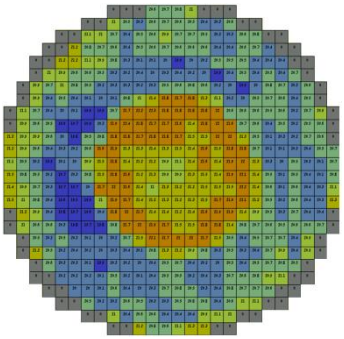

METROLOGY

The focus in Focus at IZM-ASSID are investigations of 3D-Features e.g.:

- high speed bump height measurements
- high accurate TSV-depth measurements
- layer characterization (thickness and profile) in reference to process flow
- 3D failure analysis for hidden structures (e.g. TSV-copper fill; interconnects of multi die stacks)

The following metrology services are offered by Fraunhofer IZM-ASSID:

Bump Height Measurement

- white light triangulation
  - bump height 7-80 µm
  - up to 25 million bumps per wafer
- high throughput measurement (max. 15 wph)
- automated 4'' - 12'' wafer handling

TSV-depth Measurement

- interferometric depth measurement
  - 1µm up to 300 (confocal: 700µm)
- up to 12'' wafer

Defect Inspection

- automated defect inspection (AOI)
  - min. defect size 1 µm-5 µm (depends on structure complexity and contrast)
- automated 4'' - 12'' wafer handling & film frames

Topology

- confocal microscopy
  - 5 nm surface topology @ mag 20x (higher accuracy for opaque materials)
- up to 12'' wafer

Layer Thickness

- ellipsometry (thin layers):
  - 5-2000 nm Oxid / 5-150 nm Nitrid
  - polymer <5 µm
  - layer stack with up to 3 layers
- interferometric layer thickness measurement (thick layers):
  - transparent layer stacks with single layer thickness of >1µm
- sheet resistance measurement (metal layer):
  - 5 nm-10 µm metal thickness
- up to 12'' wafer

Wafer Thickness & Bow / Warp (VIS)

- 2 white light sensors (chromatic distance measurement)
  - wafer thickness 20-5000 µm
  - measurement resolution 0.1 µm
- up to 12'' wafer
- wafer thickness, TTV, TIR, wafer warpage & bow

Wafer Thickness (infrared)

- chromatic infrared sensors
  - wafer thickness in silicon 20-300 µm
  - Measurement resolution <1 µm
- up to 12'' wafer

Die Warpage Measurement

- confocal laser profilometer
  - Measurement range: ≥ 1mm
  - Lateral resolution: ≥ 1µm, z ≥ 100nm

Physical Failure Analysis

- X-ray tomography
  - Detail recognition: ≥ 0.5 µm
- up to 12'' wafer & samples up to 400x400x50 mm
- void localization & 3D-stack inspection

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