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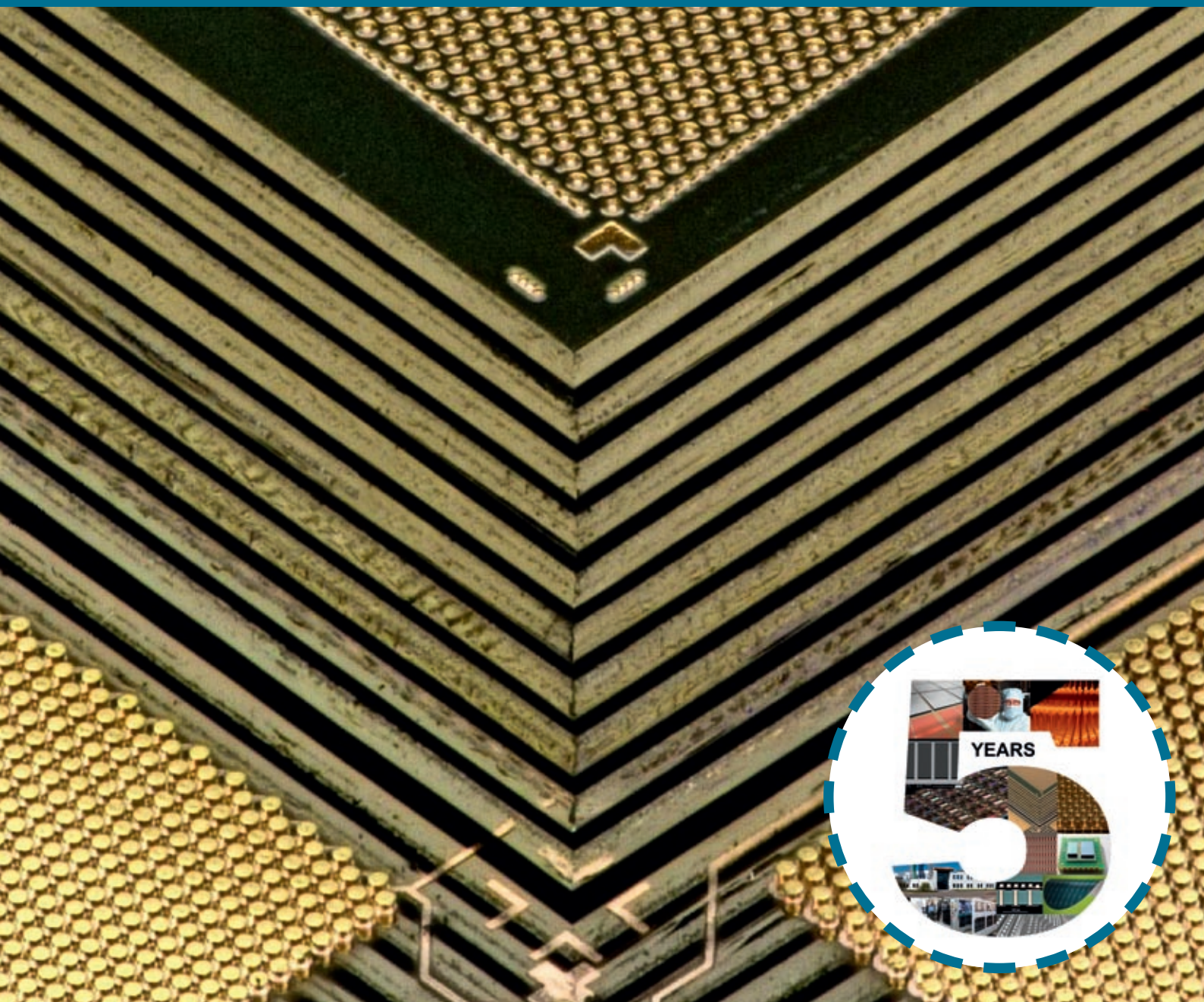
FRAUNHOFER INSTITUTE FOR RELIABILITY AND MICROINTEGRATION IZM

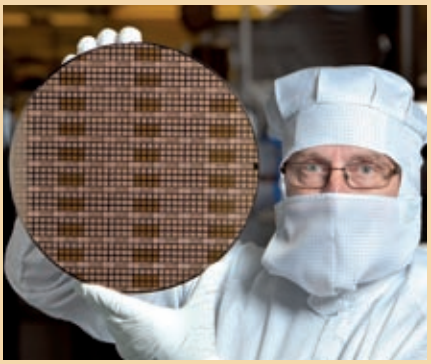
FRAUNHOFER IZM – ASSID
ALL SILICON SYSTEM INTEGRATION DRESDEN



ALL SILICON SYSTEM INTEGRATION DRESDEN FRAUNHOFER IZM-ASSID

FRAUNHOFER IZM

The Fraunhofer Institute for Reliability and Microintegration (IZM) is one of the 12 institutes of the Fraunhofer Group for Microelectronics. The Fraunhofer-Gesellschaft is one of the leading organizations of applied research in Europe undertaking contract research on behalf of industry. Fraunhofer IZM is a worldwide renowned institute specializing in developing advanced packaging and system integration technologies and transferring research results to the industry and thus being able to offer customer-specific solutions for microelectronic products in the overall scope of smart system integration.



FRAUNHOFER IZM-ASSID

The center "All Silicon System Integration Dresden – ASSID" operates Fraunhofer IZMs leading edge, industry-compatible 200/300 mm 3D wafer-level process line with modules for TSV formation, TSV post-processing, pre-assembly, wafer-level assembly, stack formation and with related metrology tools. ASSID is focusing on process development, material and equipment evaluation as well as R&D services. It is a partner in national, European and worldwide industrial and scientific networks for 3D system integration, e. g., ITRS, ENIAC, Catrene, EPOSS, Euripides, SEMATECH and Silicon Saxony. Fraunhofer IZM-ASSID has established cooperation and joint development programs with industrial partners for undertaking material and equipment evaluation, process development as well as process and product integration.

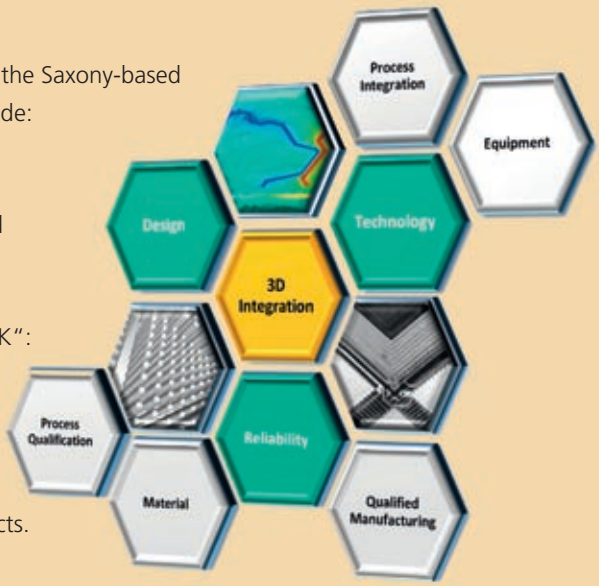
COOPERATION ACTIVITIES

Within the realms of academia, IZM-ASSID is cooperating with

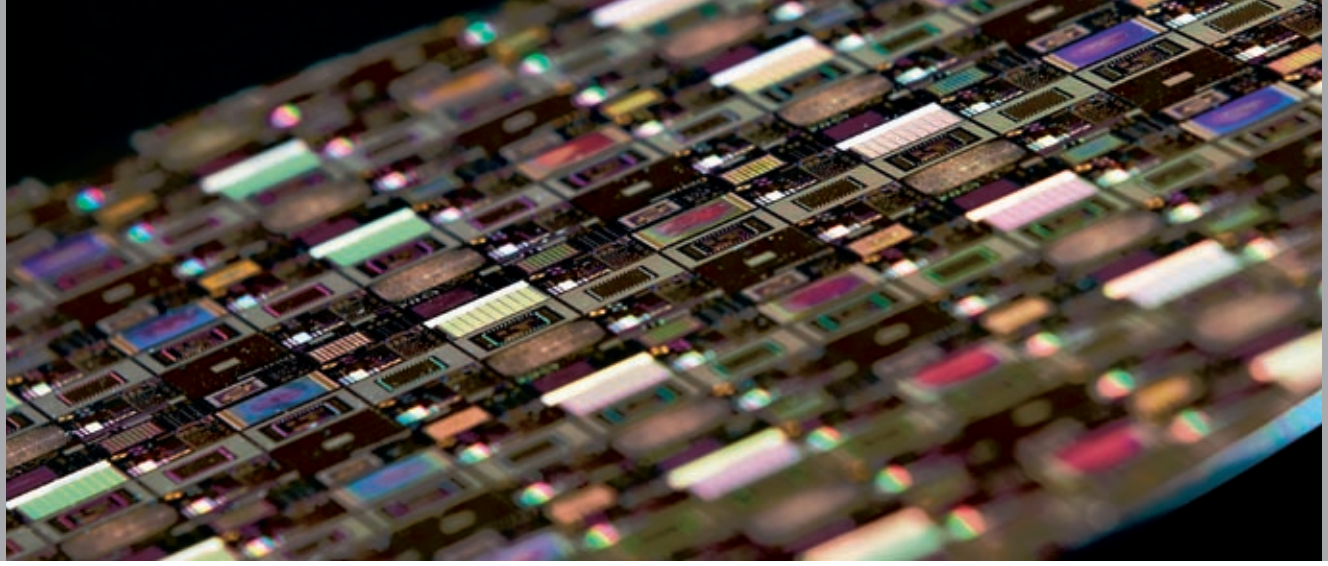
- Technische Universität Dresden (Electronic Packaging Laboratory, IAVT) and
- Technische Universität Chemnitz

Fraunhofer IZM-ASSID has established close collaborations especially among the Saxony-based Fraunhofer Institutes. Besides joint projects and services, these activities include:

- FRAUNHOFER CLUSTR 3D INTEGRATION: To cope with the technological complexity of 3D integration, leading Fraunhofer institutes cluster their outstanding competencies in the fields of technology, design, analytics and reliability to cover a broad spectrum of topics and approaches. www.3D-integration.fraunhofer.de
- LEISTUNSZENTRUM „FUNKTIONSINTEGRATION MIKRO-/NANO-ELEKTRONIK": Fraunhofer, TU Dresden and TU Chemnitz cluster their competencies in the fields of micro/nano electronics and thus strengthen the competitive and innovative capacity of the Free State of Saxony. Research know-how will – in close cooperation with resident companies – be extended and innovations can be implemented more quickly into applications and products.



Cover picture: 3D chip stack (10x) with Cu-TSVs

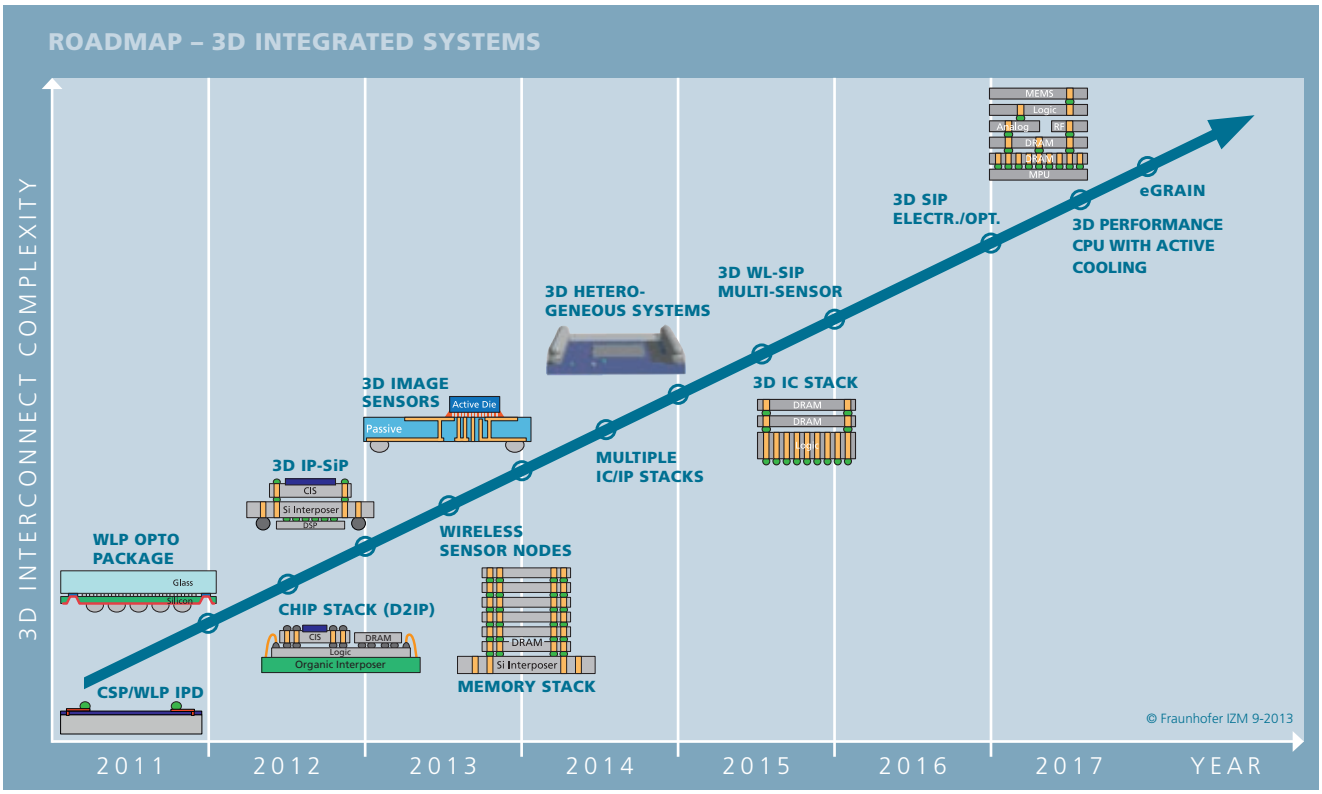


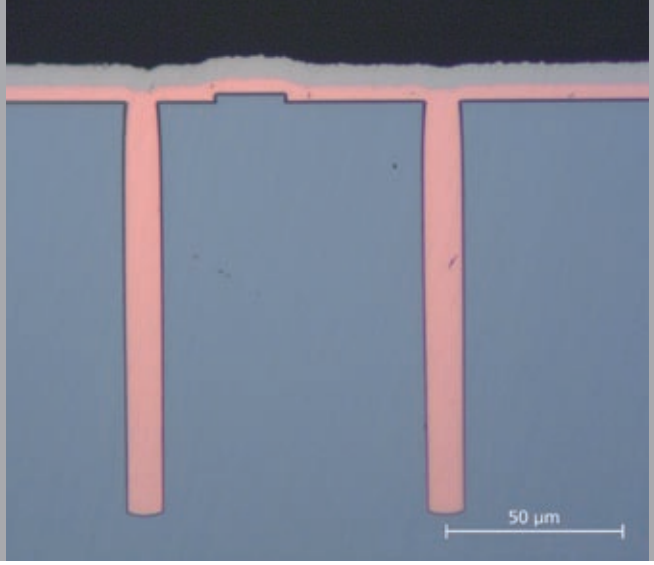
HETEROGENEOUS 3D WAFER-LEVEL SYSTEM INTEGRATION

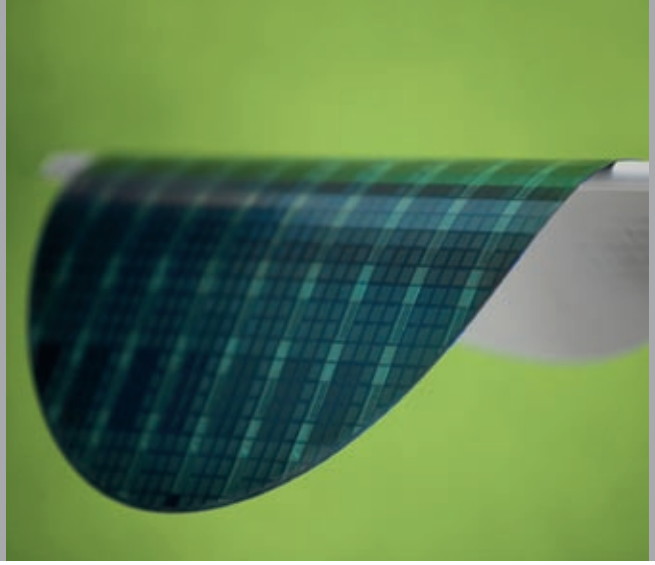
3D integration is of high significance for the realization of future innovative products and a key enabler to deal with the technical requirements e.g., performance, form factor and functionality for smart systems in different application fields like information & communication, security, healthcare, mobility & transportation and industrial electronics. It allows the multi-device integration of sensors, processors, memories and transceivers into one optimized wafer-level system-in-package (WL-SiP). Therefore, scientific and industrial research is focusing on developing 3D integration technologies to enable 3D smart systems.

Core Competencies:

- Leading-edge micro-electronic packaging
- 3D heterogeneous system integration
- Wafer-level System-in-Packages (SiP)
- Enhanced interconnection & assembly technologies
- Customized technology development
- Customer-specific prototyping & pilot-line manufacturing
- Process transfer & product integration
- Process, equipment & material evaluations as well as qualification







COPPER THROUGH SILICON VIA (TSV) FORMATION

Through silicon Vias (TSVs) are a key element in 3D wafer-level system integration. Fraunhofer IZM-ASSID has developed a TSV process (POR) for customer-defined applications based on Cu-ECD.

All processes are carried out using leading-edge, industry-compatible process equipment for 200/300 mm wafers.

Capabilities and research focus:

- High-density Cu-TSV technology (via-last, via-middle, backside via-last) for active circuit devices and interposers
- Application-specific TSV dimensions diameter/depth:
  … min. 5 µm/50 µm
  … typ. 10 µm/120 µm
  … 20 µm/120 µm
  … backside TSV (Cu-liner) up to 250–700 µm depth
- Cu-TSV filling using high-speed ECD
- Evaluation and qualification of new materials for isolation, barrier/seed and TSV filling
- Optimized via reveal

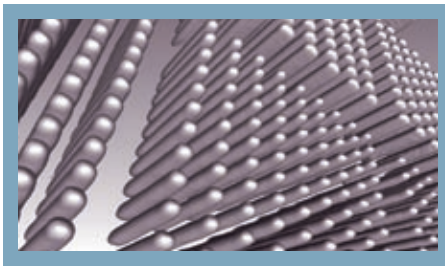
WAFER THINNING, AND THIN WAFER HANDLING

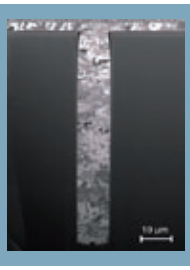
Wafer thinning and thin wafer handling technologies are an integral part of the TSV process integration as well as essential for the realization of 3D system architectures.

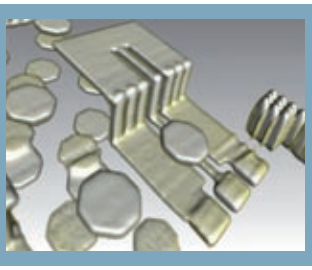
Continuous optimization of these technologies is indispensable to meet the requirements of cost-effective manufacturing and the realization of 3D systems.

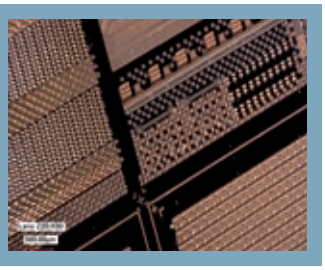
Capabilities and research focus:

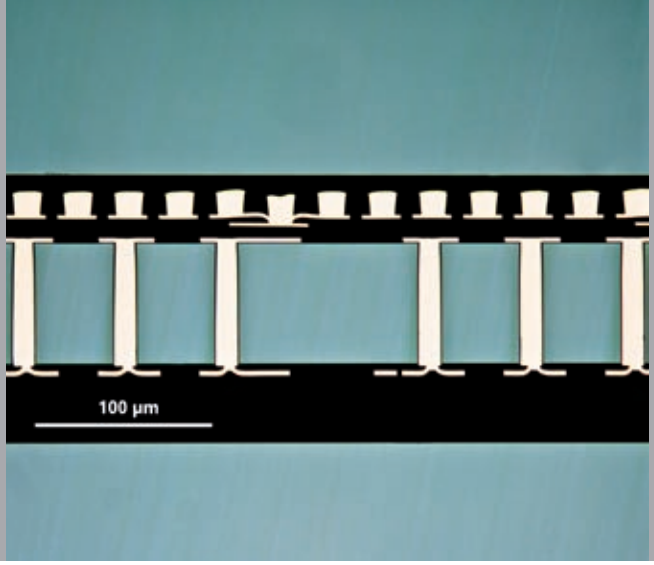
- Optimization of temporary wafer-bonding and de-bonding technologies (device wafer thickness: > 20 µm; multiple repeatable bonding and de-bonding processes)
- Enhanced wafer thinning and stress relief technologies for ultra-thin wafers (> 20 µm)
- Enhanced dicing technologies using low k-materials, small dicing streets (< 40 µm) and reduced mechanical edge and corner damage to wafer frontside and backside

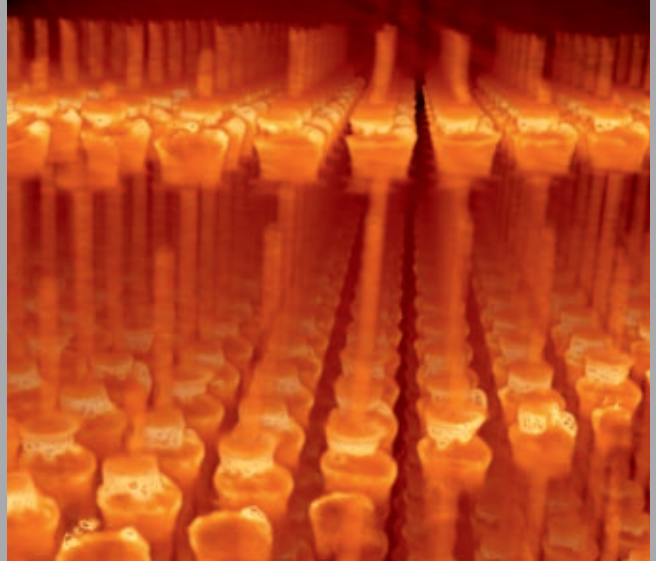












TSV-INTERPOSER WITH HIGH-DENSITY REDISTRIBUTION

The TSV interposer is used as a carrier to meet the technical specifications of integrated circuits e.g., geometry, high number of I/O and their high-density routing. According to the application, multi-layer high-density wiring on frontside/backside down to < 2 µm line/space as well as Cu-TSVs with diameters between 5–20 µm are required. The functionality of Si-interposers will be extended by the integration of passive devices such as inductors, resistors and capacitors – with an emphasis on RF applications. Next generations will also include integrated active devices and deal with high power dissipation by applying innovative cooling architectures and will also address the integration of electrical/optical interconnects for high speed data transmission. These new generations of Si-interposers are the basic prerequisite for modularized 3D stacked architectures for fully heterogeneous system integration.

Capabilities and research focus:

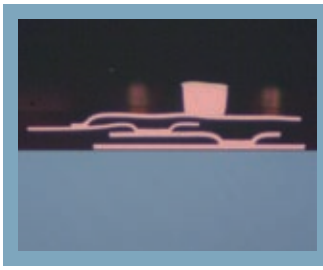
- Interposers with high-density Cu-TSV
- High-density multi-layer copper wiring: > 2 µm line/space, 4-layer frontside RDL, up to 3-layer backside RDL
- Integration of passive devices (R, L, C)
- Embedding of active and passive devices
- Interconnects for 3D stacking of devices/substrates
- Thermal management

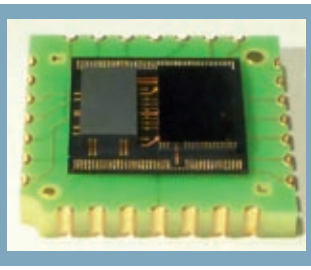
ASSEMBLY AND INTERCONNECTION TECHNOLOGIES

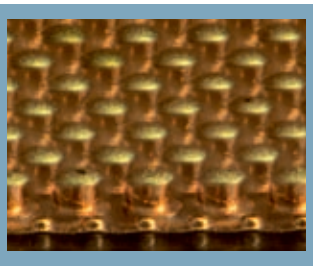
Assembly and interconnection technologies relevant for 3D system integration are strongly affected by IC technology nodes. Key parameters include die size, number of I/O, pad geometries, passivation layers, wafer-surface topologies, terminal pads and limitations to the thermal budgets that can be applied during assembly. Additional challenges in assembly and interconnect technologies for 3D systems include alignment accuracy, yield requirements and productivity that meet the demands of cost effective manufacturing.

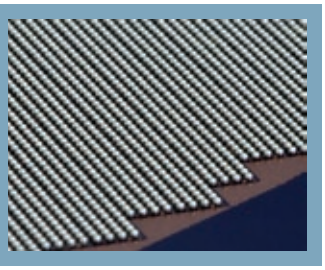
Capabilities and research focus:

- Evaluation of die-to-wafer (D2W), die-to-interposer (D2IP) and wafer-to-wafer (W2W) assembly technologies
- 3D IC assembly with high-density interconnects (> 1000 I/O) and ultra-fine pitch (> 50 µm)
- IC assembly with thin and ultra-thin chips (20–150 µm)
- Evaluation of low-temperature assembly technologies
- Evaluation of flux-free solder connections with self-alignment capability
- 3D stack formation









CUSTOMER SERVICES

3D Wafer-level System in Package Pilot Line

Fraunhofer IZM-ASSID provides prototyping and low-volume manufacturing services (300/200 mm) at its leading-edge pilot line for wafer-level packaging. Fraunhofer IZM-ASSID has established strong cooperations with leading material and equipment suppliers in which customer-specific solutions in the fields of material, equipment and processes are developed and introduced into products. As a member of the Fraunhofer Cluster 3D Integration, Fraunhofer IZM-ASSID offers – together with its Fraunhofer partners – fully customized support for 3D integration including design, technology and reliability.

Technological services include:

- Customer-specific prototyping (WL-SiP, TSV interposer) and pilot line manufacturing
- Material and equipment evaluation, process development, process transfer and product integration
- TSV silicon interposer development
- 3D TSV via middle/via last process integration
- Deposition & patterning of dielectric polymers and metal films
- Multi-layer Cu redistribution with customer-specific terminal pad metallurgies (Cu, Cu/Ni/Au, Cu/SnAg)
- Wafer thinning and thin wafer processing
- WL bumping (Cu-Pillar, SnAg, CuNiAu)
- WL solder ball attach (100 – 500 µm)
- WL assembly (D2W, W2W) and package assembly

Fraunhofer IZM-ASSIDs ISO 9001 certified management system guarantees high quality standards for its industrial services.

Fraunhofer IZM-ASSID is supported by the Federal Ministry of Education and Research, the Free State of Saxony and the European Commission.

Bundesministerium für Bildung und Forschung

Freistaat SACHSEN

Europa fördert Sachsen. EFRE Europäischer Fonds für regionale Entwicklung

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