Fraunhofer IZM
All Silicon System Integration Dresden
Scope

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All Silicon System Integration - ASSID
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Fraunhofer IZM – Focus of Activities

Materials, Reliability & Sustainable Development
- Micro Materials
- Environmental Engineering

Wafer Level Integration Technologies
- Wafer Level Packaging & High Density Interconnects
- All Silicon System Integration - ASSID

Substrate Integration Technologies
- System Integration & Interconnection Technologies
- PCB Soldering Training/Qualification and Micro-Mechatronics

System Design
- System Design & Integration

- Material characterisation
- Process evaluation
- Reliability testing
- Failure analysis
- Sample production
- Training courses
3D System Integration: Key Enabling Technologies

- 3D SiP Architecture
- Design - electrical, thermal, mechanical (DfT, DfM, DfR)
- TSV Formation (via first, middle, last (from BS)
- Interposer with TSV and multilayer RDL (FS/BS)
- Passive Device Integration
- Interconnect Formation (electrical, optical)
- Thin Wafer Handling
- Temporary and permanent Wafer Bonding
- Assembly & 3D Stack Formation
- Die-to-Die (D2D) Interconnect & Bonding for stack formation
- Heterogeneous Device Integration (MEMS)
- Test
Core Competencies

3D Wafer Level System Integration

- Through Silicon Via (TSV) Formation
- Wafer Thinning, Thin Wafer Handling
- TSV Interposer with High-density Metallization
- Assembly and Interconnection Technologies
Through Silicon Via (TSV) Formation

- High-density TSV technology for advanced system performance
- Via-middle/Via-last process integration
- Cu-TSV filling using high-speed ECD
- TSV post processes on wafer front and back side
- Evaluation and validation of new materials for TSV filling and isolation
- High yield TSV process integration
TSV Interposer with high-density Multi-Layer Metallization

- Silicon Interposer with high-density Cu-TSV
- Both sided high-density multi layer Cu-wiring
- Integration of active and passive devices in silicon interposer
- Compatible interconnects for 3D stacking of silicon components for wafer level assembly (D2W, W2W) and package/board-assembly
Pre-Assembly

- Wafer thinning and stress relief technologies for ultra-thin wafer (< 20 μm)
- Optimization of temporary wafer bonding and debonding technologies
Assembly and Interconnection Technologies

- Evaluation of die-to-wafer (D2W) and wafer-to-wafer (W2W) bonding for 3D stack formation
- 3D IC assembly with high-density interconnects (> 1000 I/O) and ultra-fine pitch (< 50 μm)
- 3D IC assembly with thin and ultra thin Chips (20 –150 μm)
3D Heterogeneous System Integration @ Fraunhofer IZM

Fraunhofer IZM- ASSID operates a Leading Edge 200/300 mm Process Line for Wafer Level System Integration for process development, prototyping and manufacturing under industry-compatible conditions.

**Facility & Infrastructure**

**Clean Room:** 970 m²

**Equipment:**
- Cu-TSV Formation
- Pre-Assembly
  - Wafer Thinning, Handling, Dicing
- 3D Stacking and Assembly

All tool specifications are aligned to the requirements for specific applications and customer requests to 3D technology for TSV formation, silicon interposer and multifunctional device integration. Tools are leading edge developments of selected supplier and aligned to process development, prototyping and low volume manufacturing under industrial manufacturing conditions.
3D Wafer Level System Integration (Examples)

- 3D TPM (ASIC+TX+MEMS)
- WL Camera
- TSV Interposer (MPU+MEM)
- MEMS /ASIC Integration
- ARM Sensor
- Image Sensor
- ASIC+MEMORY
- Image Sensor (Sensor+IP+SP)
- TCI (Sensor+ASIC+TX)
TSV Via Last Integration – Process Scenario

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WLP & 3D Integration @ Fraunhofer IZM

Fraunhofer IZM vision is to integrate heterogeneous chip functionalities in one package by using enhanced 3D integration, assembly and interconnect technologies

Development of leading edge technologies for WLP & 3D-WL System Integration

Customized solutions for product integration and process transfer

Supporting equipment and material evaluation for supplier

Prototyping and manufacturing using qualified processes on a latest state of the art process line (200/300mm) for WL packaging, and 3D WL system integration.
Fraunhofer IZM vision is to integrate heterogeneous chip functionalities in one package by using enhanced 3D integration, assembly and interconnect technologies.

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THANK YOU FOR YOUR ATTENTION

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