Electro-optical circuit board with single-mode glass waveguide optical interconnects

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ABSTRACT

A glass optical waveguide process has been developed for fabrication of electro-optical circuit boards (EOCB). Very thin glass panels with planar integrated single-mode waveguides can be embedded as a core layer in printed circuit boards for high-speed board-level chip-to-chip and board-to-board optical interconnects over an optical backplane. Such single-mode EOCBs will be needed in upcoming high performance computers and data storage network environments in case single-mode operating silicon photonic ICs generate high-bandwidth signals [1]. The paper will describe some project results of the ongoing PhoxTroT project, in which a development of glass based single-mode on-board and board-to-board interconnection platform is successfully in progress. The optical design comprises a 500 µm thin glass panel (Schott D263Teco) with purely optical layers for single-mode glass waveguides. The board size is accommodated to the mask size limitations of the fabrication (200 mm wafer level process, being later transferred also to larger panel size). Our concept consists of directly assembling of silicon photonic ICs on cut-out areas in glass-based optical waveguide panels. A part of the electrical wiring is patterned by thin film technology directly on the glass wafer surface. A coupling element will be assembled on bottom side of the glass-based waveguide panel for 3D coupling between board-level glass waveguides and chip-level silicon waveguides. The laminate has a defined window for direct glass access for assembling of the photonic integrated circuit chip and optical coupling element. The paper describes the design, fabrication and characterization of glass-based electro-optical circuit board with format of (228 x 305) mm².

Keywords: optical backplane, optical interconnect, optical graded index waveguide, micro-optics, thin glass, optoelectronic devices, silicon photonics

1. INTRODUCTION

Optical interconnects for data transmission at board level offer significant reduction in power consumption, increased energy efficiency, system density and bandwidth scalability compared to purely copper driven systems. So far such embedded optical architectures do not exist in data center and network systems, yet. However there is a clear need to replace the electrical signal lines by optical interconnects for increased high-speed data transmission due to the higher bandwidth by length product of optical interconnect structures in the backplane and line cards [2]. The system enclosure consists of different peripheral line cards that are plugged into an electro-optical backplane where signals are routed across. The integration of optics to the line cards can be divided in three possible configurations as shown schematically in Figure 1. Line card A has an optical engine closely located to the integrated circuit in order to convert high speed electrical signals into optical signals for data transmission through the system by flexible optical signal links. On line card B the flexible optical links are replaced by rigid integrated waveguide layers. Line card C (blue frame) shows a configuration in which electrical IC and optical engine are merged to a photonic IC. Such configuration C will be proposed in the following chapters. It can be feasible by silicon photonic ICs having single-mode waveguides working at 1310/1550 nm on IC level.

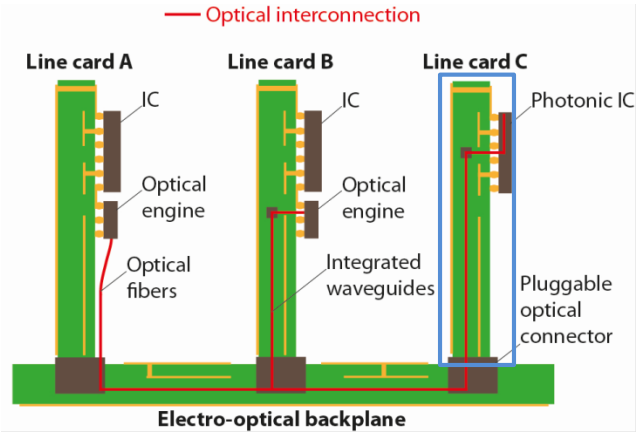

Figure 1: Schematic for board-level optical interconnection (red line) which consists of an electro-optical backplane with integrated waveguides, pluggable optical board-to-board connectors and three possible line card configurations with A) flexible optical fiber or B,C) integrated waveguide links. Optical engines on different line-cards are optically interconnected (red line) over optical fiber links on the line card, or pluggable optical board-to-board connectors on electro-optical backplane with integrated waveguides.

Silicon photonics offers unique bandwidth possibilities because of wavelength division multiplexing. For that multiplexing, board-level optical interconnects have to be single-mode. Today, worldwide research focuses on implementing all important photonics building blocks in silicon like such as the laser, modulator, switch, filter, and detector. On the other hand, there is a lack of single-mode optical interconnection between silicon photonics devices assembled on printed circuit boards (PCB). Our ongoing research activities comprise the development of a single-mode printed circuit board PCB for fabrication of optical line-cards and backplanes. Also in progress is the development of optical coupling interfaces to photonic ICs and pluggable optical connectors. Fraunhofer IZM is targeting to develop a single-mode electro-optical circuit board (EOCB) for high-precision flip-chip assembly and e/o interconnection of silicon photonics components and optical interconnection with single-mode optical fibers.

2. A NEW PACKAGING CONCEPT

The electro-optical interface between silicon photonic components and underlying substrates is not standardized and different research approaches have been reported in the past [3][4][5]. Our packaging concept consists of planar glass waveguides and electrical pads patterned on glass. Our new approach is the automated alignment of a silicon photonic interposer directly above a manufactured cut-out area in the optical glass layer. Furthermore, a coupling element will be assembled underneath in the glass cut-out and in front of the waveguide facet for optical interconnection between the optical ports of the silicon photonic interposer and the glass waveguide array. The board-to-chip interface consists of a free space optical path with a concave mirror element for beam deflection and refocusing of the signal as shown in Figure 2.

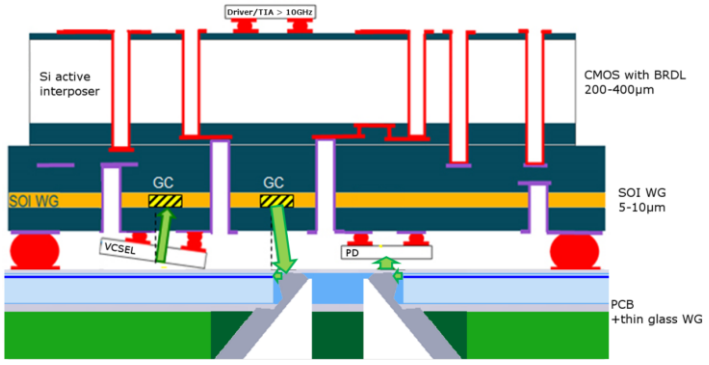

Figure 2: Schematic of the electro-optical interface between the silicon photonic interposer and the electro-optical circuit board; in the lower half in dark green and bright blue are the cavities structured to integrate the coupling element (white) and the mirror (grey) into the EOCB with waveguides (dark blue) guided below the upper glass surface.

The photodetector and laser will be hybrid-integrated on the silicon photonic interposer. An array of vertical-cavity surface-emitting lasers (VCSELs) and photodiodes are flip-chip assembled on the interposer's bottom side. The light of the VCSELs is coupled by grating couplers into the silicon-on-insulator (SOI) waveguides. In our concept, grating couplers are the optical I/Os for interconnection with the EOCB. Additionally, backside illuminated flip-chip assembled photodiodes underneath the interposer will be also be receiving optical signals for O/E conversion. The active area of the photodiodes is not on the same focus level as the grating couplers—a fact that has to be considered for the packaging concept. Additional ASICs can be mounted on the top side of the interposer and electrical signals are routed by through-silicon vias (TSVs).

The glass is the core layer in the electro-optical circuit board (EOCB) stack-up. The transparency, thermal stability and low CTE are the main benefits for promoting the concept of embedding a glass layer into a printed circuit board. Windows in the stack-up above and underneath the glass layer provide access from both sides to the glass core layer for assembly on glass. An EOCB was designed to proof out our concept and evaluate the necessary technologies for fabrication. The board size was defined to (233 x 303) mm², having two areas for silicon photonic interposer assembly as shown in Figure 3. The 500 µm glass layer with optical waveguides (turquoise lines) and electrical circuitry (rose lines) has an area of (84 x 181.5) mm² and is embedded as the core layer between FR4 prepregs (green) and patterned copper (rose lines) layers. On the four sides around the functional glass layer, the optical interfaces are defined for board-to-board and fiber-to-board waveguide termination.

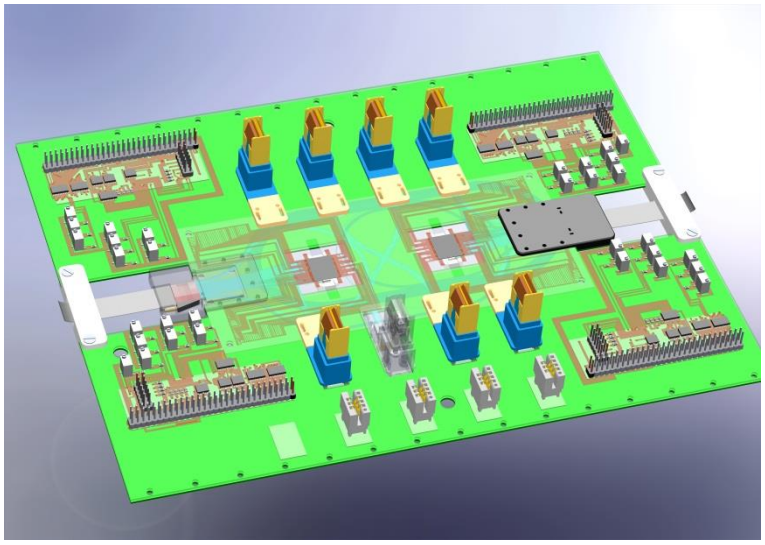

Figure 3: Concept view through the assembled EOCB with optical waveguides (turquoise lines), electrical circuitry (rose lines) and prepreg and FR4 layers (green).

The PhoxTroT single-mode EOCB demonstrator platform contains an electro-optical backplane with two optical router chips on it. Up to four electro-optical line cards with transceiver chips can be plugged into the slots and optical interconnected over the electro-optical backplane. Two V-Groove-Arrays with 96 fibers each are coupled with the electro-optical backplane, and can be leaded to through the 96 optical connectors on the back of the case. The router chip can be remotely controlled via a SPI interface, which is connected via electrical control-headers. For high frequency measurement are arranged some electrical prober needle pads, located very close to the router chip for testing and characterization. A side and top view of the full arrangement is depicted in Figure 4a and b. The demonstrator is cased in a standardized chassis, as Figure 4c shows. It is a sub-rack with 19"-formfactor and a height of 7 units. It contains a retractable power supply and some cooling fans. There are four line card slots, easily to serve from the front. To remove the backplane it's necessary to open the back cover. The backplane has five electrical and one optical layer. The width of 233 mm is deriving from the Euro-card form factor (6 units) which is even used for the line cards. The board length of 303 mm allows placing all needed parts on board and leaves enough space in the chassis for wiring. The maximum board thickness has to be less than 3 mm, as the laser direct imaging (LDI) system for EOCB fabrication currently in use doesn't support thicker boards. Two lateral rows of 2.7 mm diameter holes, pitched 15.24 mm, and 4.825 mm distance from the edge, are used to screw the backplane into the chassis.

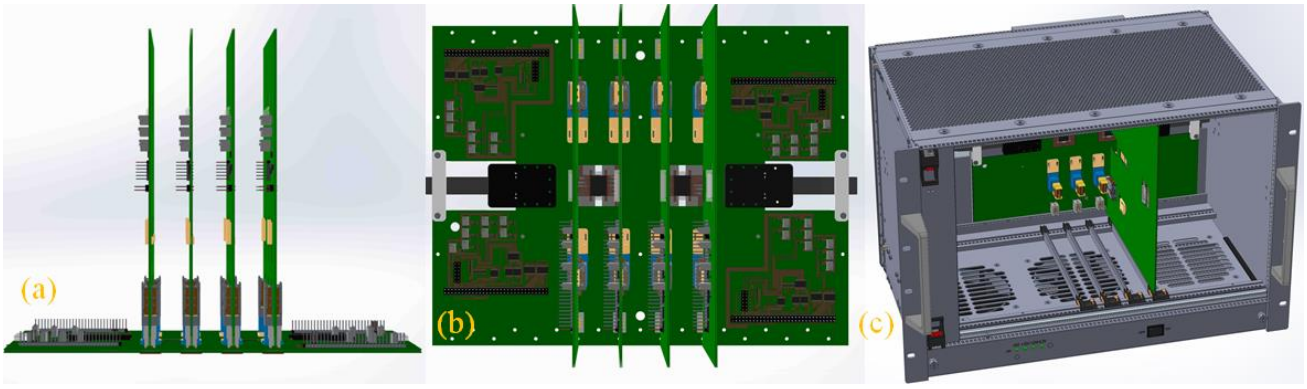

Figure 4: a) side and b) top-view on optical backplane with four insert line-cards, c) backplane and one plugged line-card mounted in 7U chassis.

3. ELECTRO-OPTICAL CIRCUIT BOARD FABRICATION

A 200 mm wafer-level process was selected for development of optical and electrical integration of interconnects on glass. A two-step thermal silver ion-exchange waveguide process has been applied for planar waveguide integration. The refractive index profile is characterized by an elliptical cross section with the index a maximum in the waveguide center 5 µm below the glass surface [6]. The waveguide layout is defined by an aluminum thin-film mask. The mask opening width directly influences the lateral waveguide dimensions. Lithography and wet-chemical etching is applied to defining the waveguide layout with mask openings of 3 µm. The process is performed on at the wafer level because of the resolution limitation of our in-house laser direct-imaging (LDI) system (the Orbotech Ultra-200 with 8 µm line width and 12 µm spacing). Improving panel-level lithography for this system is being currently under investigation. A 5 µm PVD glass cladding layer was deposited over the full area as an optical cladding layer. A 7 µm CTE compensation layer made of polyimide was patterned in the area between the electrical copper lines and the glass. Then the electrical circuit was patterned by thin-film metallization with copper lines of 5 µm height. For increasing the distance between the glass and the silicon photonic photonic interposer, and for the underneath flip-chip assembled components, 50 µm copper pillars with bondable surface finish were additionally patterned on glass for the interposer attach process. The manufactured wafer is shown in Figure 5 with dual-layer embedded single-mode waveguides on both sides and electrical circuitry with bond pads on one side. (In the presented demonstrator the top optical layer is used only.) Finally, the glass wafer was cut to smaller panels of (84 x 181.5) mm² in size, and two cut-out inserts between the electrical pad rows were created for later placement of the optical mirror underneath the silicon photonic interposer.

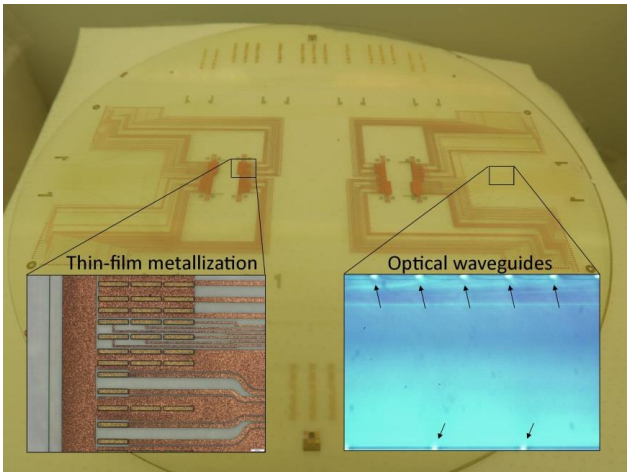

Figure 5: Optical dual-layer waveguide integration and thin-film metallization on a 200 mm wafer level.

The resulting glass panel (84 x 181.5) mm² is embedded as an inlay in a pre-prepared glass frame (233 x 303) mm² for achieving a full area symmetrical PCB stack-up. The glass frame was precisely processed by laser cutting. For the frame,

glass was selected instead of FR4, which showed high warpage of the EOCB after lamination due to the CTE mismatch. Provided cavities in the four corners of the glass frame were filled with FR4 inlays of the same size to allow through via drilling with standard mechanical PCB equipment without destroying the glass. By using this process, and also because of the use of copper plating of the through-vias, benefits accrue because a standard chemical pre-treatment for copper plating is used instead of the need for depositing an adhesive layer inside the vias. Copper circuits were successfully patterned on different stack-up materials like such as glass, FR4, and prepregs and were interconnected by vias as shown in Figure 6.

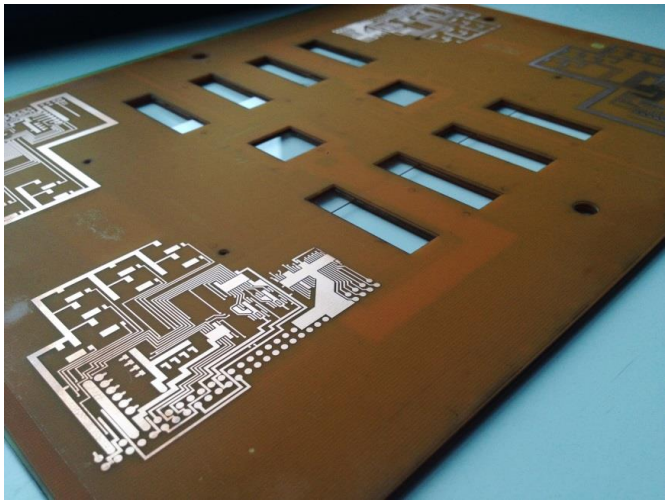

Figure 6: An electrical PCB with an embedded optical glass layer (EOCB).

4. SILICON INTERPOSER ASSEMBLY

The optochips employed in the frame of Phoxtrot consist of 100 µm thin Silicon photonic interposers on which active add-ons as VCSEL, photodiodes (PD), transimpedance amplifier (TIA) and drivers are assembled. Gold-Gold (Au-Au) thermocompression (TC) bonding [7] has been chosen as the assembly technique for the assembly of active add-ons to the photonic interposer as well as for the assembly of the interposer to the EOCB. Using Au-Au TC bonding enables reaching high post-bonding accuracy of ±1 µm, which are required for the PhoxTrot concept in order to obtain optimum coupling efficiencies.

First, the active add-ons are being assembled to the photonic interposer: Aluminum bonding pads of the the photonic interposer have been stud bumped to enable Au-Au TC bonding. VCSELs and PDs have gold contacting pads and can therefore be directly assembled to the bumps. TIAs and drivers have Al pads and also need to be bumped before being assembled to the photonic interposer. In Figure 7, microscope pictures of some of the assembled components are shown:

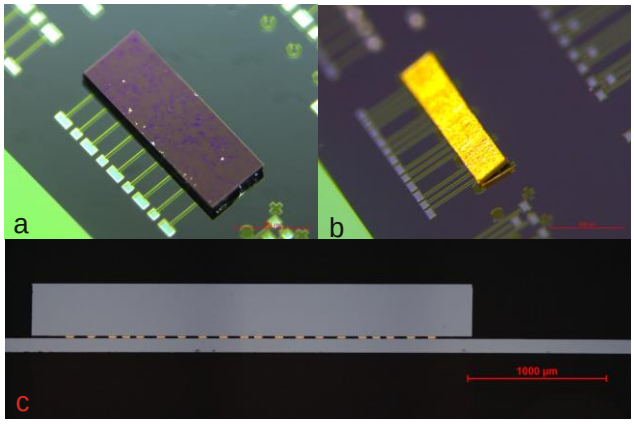

Figure 7 a) Stereo microscope picture of PD bonded to silicon interposer b) Stereo microscope picture of VCSEL bonded to silicon interposer c) Cross-section of drivers bonded to silicon interposer

In Figure 7b, it can be seen that the VCSEL has been assembled with an angular tilt. The reason for this is that the light emmited by the VCSELs on the router optochip will be coupled to the waveguides via a grating coupler. Optimal coupling efficiencies are obtained when the laser beam has an incident angle of 10° with respect to the direction normal to the grating coupler. In order to bond a VCSEL with a 10° tilt, a tilted flip-chip bonding process has been developped. The obtain such a tilt, a combination of single stud bumps and double stacked stud bumps is used. The VCSEL is then TC bonded by means of a special bonding tool in order to be placed with the desired tilt. This tilted flip-chip process has been patented (German patent granted and US patent pending). In Figure 8, a cross-section of a VCSEL bonded with a 10° angle is shown:

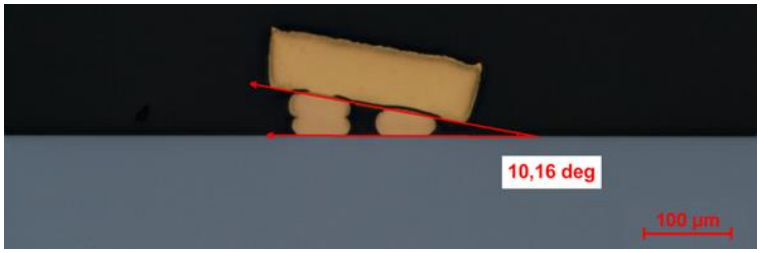

Figure 8 Cross-section of a VCSEL bonded with a 10° tilt

The measured angle corresponds well to the targeted bond angle, considering measurement imprecisions. Coupling efficiencies are currently under investigation and measured. Once the active add-ons have been assembled to the interposer, the interposer itself is assembled to the EOCB. The interposer has undergone similar processing as the glass wafers described above: 50 µm high Cu pillars have been electrodeposited on the interposer, with a finish adapted to Au-Au TC bonding. These Cu pillars are stud bumped as well in order to be TC bonded to the Cu pillars that have been deposited on glass. Special tooling has been developed in order to be able to deploy this bonding technique, due to the boundary conditions that have to be considered in this case. Since TC bonding is based on exerting pressure, the components assembled on top of the interposer need to be protected, as directly pressing them would destroy these components. Furthermore, the glass with copper pads on which the optochip is to be bonded lies in a cavity. Therefore, a support tool is used in order to avoid strong bending of the glass while TC bonding the optochip. Given typical Au-Au TC bonding pressures (250 MPa), without the presence of a support tool, glass would very likely break during the bonding process.

5. AUTOMATED ASSEMBLY ROUTINE FOR OPTICAL CHIP-TO-BOARD COUPLING

The assembly routine is defined by solder bonding of electrical components, thermocompression (TC) bonding of the silicon photonic interposer directly on glass, and active alignment and adhesive bonding of fiber-to-board and chip-to-board interfaces. Permanent coupling of single-mode optical interconnects requires a highly accurate assembly technology with sub-micron capabilities to achieve best results. The developed coupling element has 56 bidirectional optical channels, coupling from board to grating couplers, and 12 one-directional optical channels, and coupling from board to photodiodes. The priciple of coupling is to redirect and refocus the divergent outgoing ray with a concave mirror as shown in the schematic cross section in Figure 9 for the grating coupler and photodiode I/O's. The grating couplers on the silicon photonic interposer have a first order radiation angle of 10° to the plumb line. That means that the mirror face needs to be aligned in a 50°angle relative to the waveguide plane of the EOCB. The process needs to be utterly accurate in lateral positioning as well as angular positioning, because of the presence of grating couplers and waveguide facettes. Since the mirror does not offer any flat surfaces, that lie perpendicular to the optical axis of the cameras which are used for prealignment, prepositioning of the mirror is quite a challenge. A novel quick alignment process, making use of the reflective properties of the gold coated mirror, has been developed to overcome these issues.

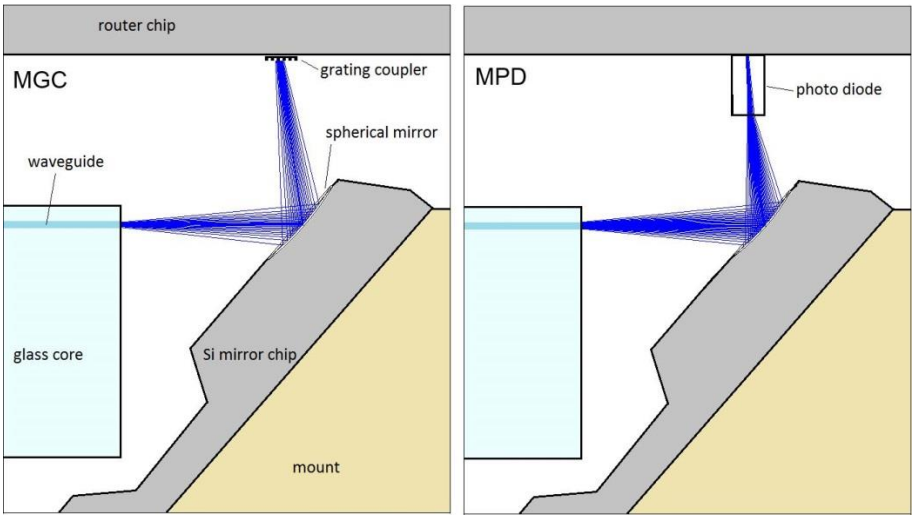

Figure 9: Deflection and refocusing of an optical beam (blue lines) between the grating coupler and glass waveguide facet (left) and photodiode and glass waveguide facet (right).

The coupling element consists of a glass mount and a silicon mirror chip. The concave mirrors were etched into a silicon wafer by combining 3D lithography and reactive ion etching. To decrease the possible distance between the mirror and waveguide facet, a ditch was etched into the chip by KOH-etching. The surface of the chip was gold sputtered for high reflectivity of the mirrors. After dicing the silicon wafer to a chip size of (5 x 15) mm², the chip was assembled by an adhesive bonding pick-and-place process to a glass mount. The assembly of the mirror element onto the glass mount requires quite accurate positioning as well as any other process step. Since both elements are passive, the advantages offered by active alignment are out of reach. To overcome that deficit a self-learning process has been implemented, to place those silicon mirrors as accurately as possible. With the mirror in the correct position glue gaps can be controlled to ±10 microns, making subsequent process steps more reliable.

One of the exceptional strengths of the developed pick-and-place process is active optical alignment, which allows finding the best possible component position making mechanical tolerances less of a factor. The basic principal here is a closed-feedback loop, which has optical characteristics as measurement parameters and axis-positions (up to 6 DOF) as the controlled condition. For waveguide arrays, the alignment becomes quite complex and requires an assembly routine which is able to cope with various starting conditions and with the huge dimensions of the coupling element vs. coupling tolerances. A precise prealignment is as improtant as the active alignment routines themselves. Since EOCBs do not provide any integrated, active optical components, the efforts for establishing an optical interconnection are quite high. The technological problem at hand requires the coupling of optical energy through grating couplers (chip-side) in and out of the integrated waveguides (board-side). Therefore, the optical signal is deflected in an 80 degree angle by the mirror of the coupling element.

The advantage of using a closed optical loop in the silicon photonics chip for active alignment of the two outer optical channels is that only one manipulation stage is needed for accomplishing the coupling task. Therefore, it will be reducing the complexity of the assembly stage, and furthermore as well as the cost of investment, as a tradeoff a more acurate prealignment is required. The developed assembling process consists of three major steps: 1) component feature detection and picking, 2) pre-alignment (by fiducials) and dispensing of adhesive, and 3) active alignment (by measuring insertion loss), including UV-curing. An assembled coupling element inserted into the glass cut-out between the electrical pad rows is shown in Figure 10.

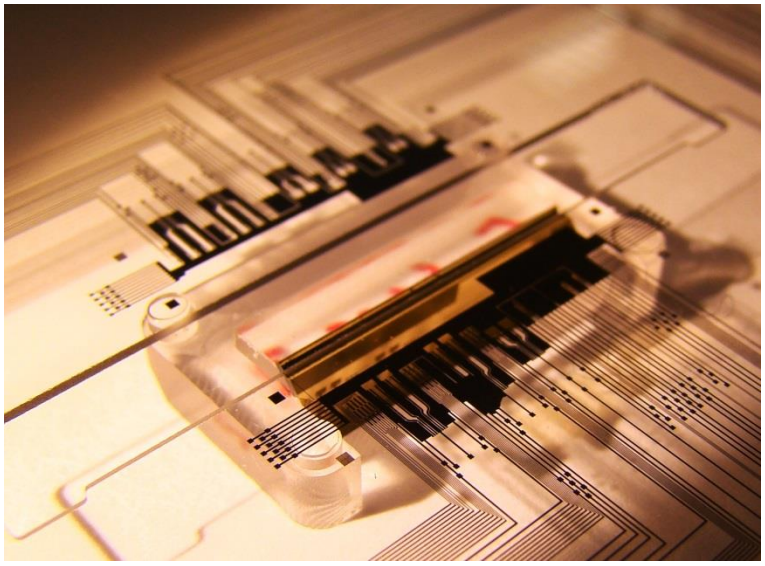

Figure 10: A coupling element fixed on the glass layer of the EOCB at bottom side. The mirror element provides a ditch to bring the spherical mirrors closer to the optical glass edge.

The combination of feature-based machine vision with high magnification telecentric camera optics, a highly precise mechanical multi-axis system, integrated optical measuring system, adaptable manipulation of components (gripping), and UV-curing adhesive, provides the flexibility which is inevitable for that kind of optical assembly approach.

6. SUMMARY

We have developed a new single-mode planar glass-based electro-optical circuit board technology providing a silicon photonic IC platform for data center and high-performance environments. A process has been presented and elaborated for fabrication and embedding of an electro-optical glass core in a PCB. Additionally, a generic optical board-to-chip coupling interface has been developed and board-level assembling technologies have been successfully proven. Ongoing work focuses on the full demonstration of single-mode EOCB with assembled silicon photonic ICs which are directly interconnected at the board-level with data rates up to 40 Gbit/s per channel.

7. ACKNOWLEDGMENTS

The research leading to these results has received funding from EU ICT within the European project PhoxTroT (Ref. 318240). Financial support is greatly appreciated.

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