



TEST CHIP DESIGN IZM-ASSID MULTI-PROJECT WAFER TC3

TC3 is a universal test chip layout which can be used for technology development and electrical characterization. The designs used are targeted for a wide range of topics in the area of 3D integration, high density interconnects, HF applications, and interconnects.

Each reticle contains sub-chips of 12.5 x 11.5 mm size. Eight sub chip variations are placed in each reticle:

Chip 1: HF structures

- Customer-specific HF test structures on front side and backside of wafer
- Daisy chains
- TSV Kelvin test structures
- Vertical coil structures

Chip 2: Cavity structures

- Large cavity
- Test structures to determine lithography process window within cavity

Chip 3: High density layout

- Experimental design for multi-layer high density redistribution layer
- Up to 4 wiring levels at 10 μm pitch
- (front side only)

Chip 4: Thermal studies

- Coils for inductive heating of TSV
- Analysis of TSV damage due to heating

Chip 5: HF structures

- Coils and transmission lines of various geometries in 4 RDL layers

Chip 6: Flip chip bonding

- Contains bond pad array of 10 mm x 10 mm size
- Design allows electrical localization of failing connections for subsequent failure analysis

Chip 7: Daisy chains

- TSV daisy chains of various designs using 10 μm TSV diameter
- Via daisy chain of various designs, via sizes from 3 μm to 10 μm

Chip 8: Comb structures

- Comb structures to characterize k-value and leakage characteristics of RDL materials

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