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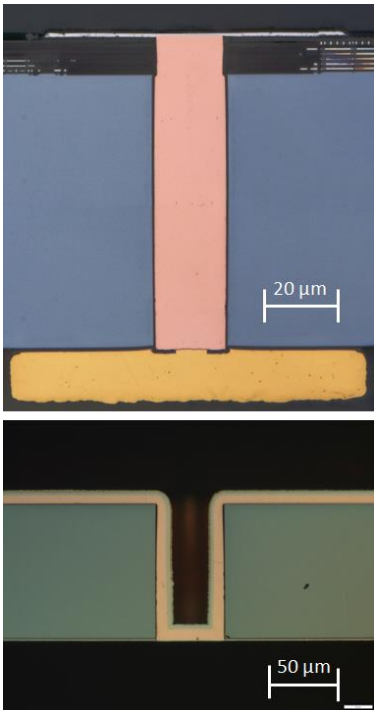

CMOS ICs with TSVs in front side via last (top) and back side via last (bottom) technology

CMOS TSV Last Integration Technologies

3D wafer level system integration is one of the most important key technologies in microelectronic packaging and system integration worldwide. This concept has specific advantages in terms on heterogeneous integration of multiple devices such as sensors, processors, memories and transceivers with excellent electrical performance and small form factor. Especially integarted cirquits with through silicon vias (TSVs) offer new possibilities to build 3D SiPs based on e.g. high pin count ASICs, memories and MEMS.

Fraunhofer IZM has developed processes for custom specific post BEOL integration of TSVs into active CMOS wafers. Depending on the product requirements and available real estate TSVs are realiszed either using a front side via last or back side via last implementation flow with a high degree of flexibility in TSV geometry and density.

In case of a front side via last implementation flow DRIE processes are used to etch blind holes with straight side walls through the BEOL and further down into the bulk silicon of the CMOS wafers. The holes are isolated by CVD and metallized by PVD for barrier and seed layer deposition followed by complete copper filling using electro-chemical deposition. Interconnections between TSVs and original chip IOs are formed by typical thin film RDL processes. The TSV blind plugs are later accessed from the back side of the wafers by silicon thinning, depositioning and opening of isolation layers as well as deposition of RDL structures or contact pads. Typical TSVs have diameters in the range of 5-20 µm and aspect rations between 5 and 10.
The upper picture shows a cross section of a 90 µm thick CMOS IC with a copper filled TSV of 18 µm diameter, front side thin film RDL and back side second level contact pad.

In case of a back side via last implementation flow straight or slightly sloped TSVs are etched from the wafer back side down to dedicated IO landing pads which are part of the BEOL metallization. After deposition and opening of isolation layers a liner metallization is processed by barrier/seed layer sputtering and electro chemical deposition to re-route the IO contacts from inside the vias to the back side of the ICs. Finally a passivation layer as well as second level IOs are fabricated at the wafer back side. Typical TSVs have diameters >=50 µm and aspect ratios < 3.
The lower picture shows a cross sectional view of a straight TSV with liner metallization in a 100 µm thick CMOS IC.

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