

Packaging is Shaping Future Electronics—

6.11.2025

Prof. Dr.-Ing. Ulrike Ganesh

Microelectronics Integration – Where do we come from and where are we going?

- Fraunhofer IZM
- Insight to the evolution and IZM's role

Technology Highlights and Roadmap Perspectives

Chiplet Integration BEoL

Chiplet Integration Backend&Assembly

Power Electronics Integration

Photonic Packaging and Co-Packaged Optics

RF (5G+, 6G) and RADAR Integration

Environmental Impact of modern electronics (Hyperscaler AI)

Future Topics

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The Fraunhofer-Gesellschaft

At a glance*

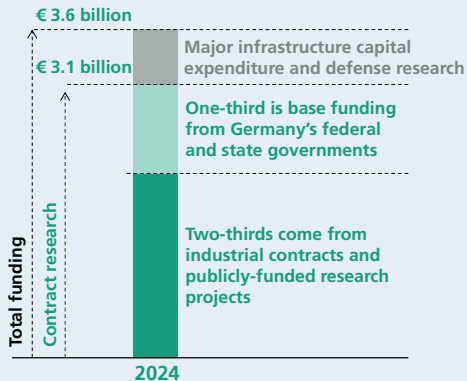
Applied research focusing on key future-relevant technologies and the commercialization of findings in business and industry. A trailblazer and trendsetter in innovative developments.



≈ 32,000 employees



75 Institutes and
Research Institutes



*The given figures relate to 2024

Research Fab Microelectronics Germany (FMD)

Fraunhofer IZM is part of the FMD*



11 Fraunhofer
2 Leibniz-Institutes

1 MES over 10 institutes
ISO9001 certified



191 First patent applications
2986 Active patent families

13 clean rooms
19,500 m² clean room space
>2,200 tools/equipment



> 4,900 Employees
Including 2,800 scientists

€ 2.2 bn. assets and investment
€ 673.3 m. budget/a
€ 272 m. industry project



*The given figures relate to 2024

Fraunhofer IZM at a Glance

Over 30 years of experience



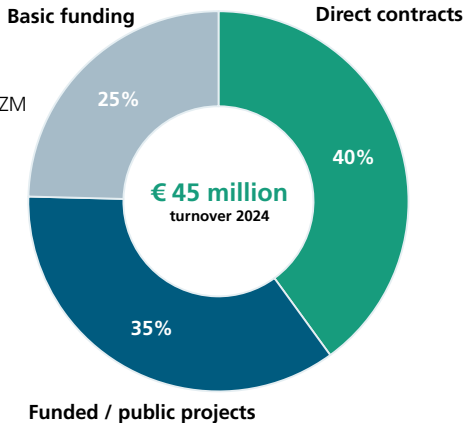
- 460 employees (including students and trainees)
- 125 interns, bachelor students, master students and student assistants have been supervised at Fraunhofer IZM
- 8 trainees



- 5,269 m² laboratory space
- 68 labs and measurement spaces



- Long-term contracts with
- Technical University of Berlin
 - Technical University of Dresden
 - Brandenburg University of Technology



Our Locations and Partnerships with Universities

Progress in microelectronics at three locations



Key Research Partnership with Universities

TU Berlin: Research Center Microperipheric Technologies

- Materials for Hetero Systemintegration (Prof. Dr.-Ing. Schneider-Ramelow)
- Design and Hetero-Integration of Micro-Electronic Systems (Prof. Dr.-Ing. Ganesh)
- Semiconductor Components and Microelectronic Systems (Prof. Dr. Jadaun)

TU Dresden

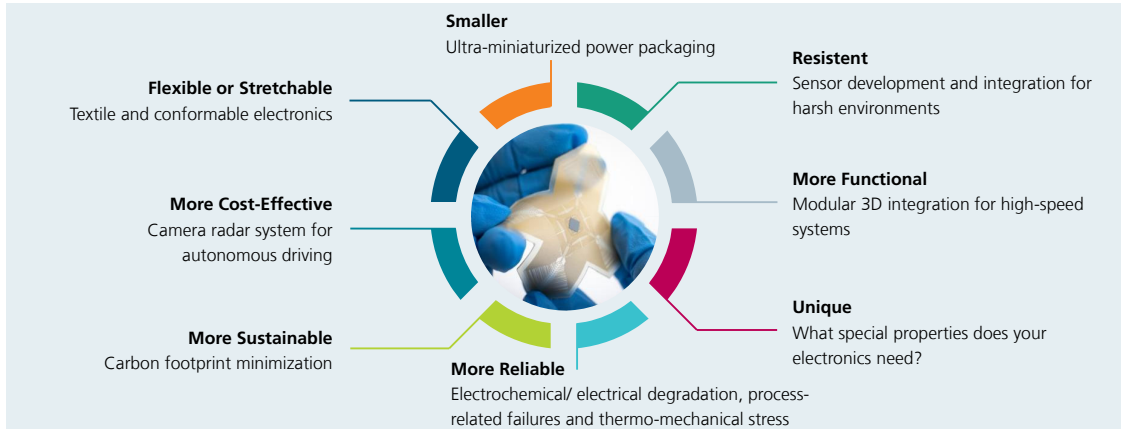
- Micro and Nano Materials for Electronic Packaging (Prof. Dr.-Ing. Panchenko)

BTU Cottbus-Senftenberg

- Antennas and High-Frequency System Integration (Prof. Dr.-Ing. habil. Ndip)

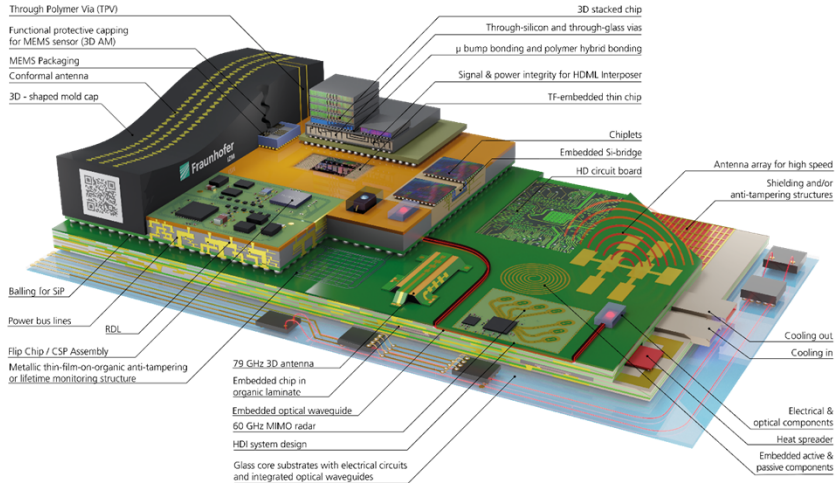


Fraunhofer IZM provides Electronics with new Properties



Our Mission at Fraunhofer IZM

Bringing microelectronics into application



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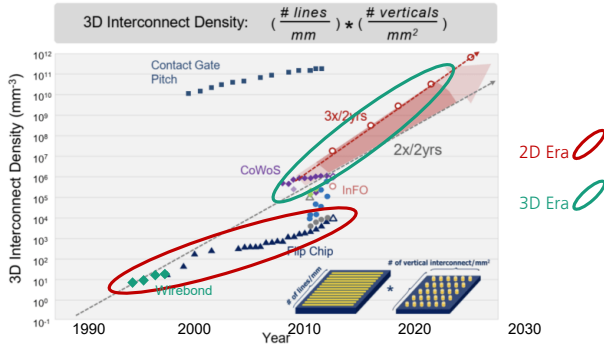
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Interconnect Density Evolution

Wirebond capability vs flip chip capability vs 3D Advanced Packaging capability



Source: D. Yu, ECTC 2020, modified by FhG-IZM

- Wirebonds, whether fine pitch or multi tier have reached their maximum integration capability
- Other 2D interconnect concepts like FlipChip or ChipScale Packages cannot follow the required (and future) I/O densities
- 3D interconnect concepts, in combination with 2D, offer a remedy to this challenge
- Combinations of 2D and 3D interconnect (like TSMC's CoWoS-S are defining the current State of the Art)

Advanced Packaging - Evolution

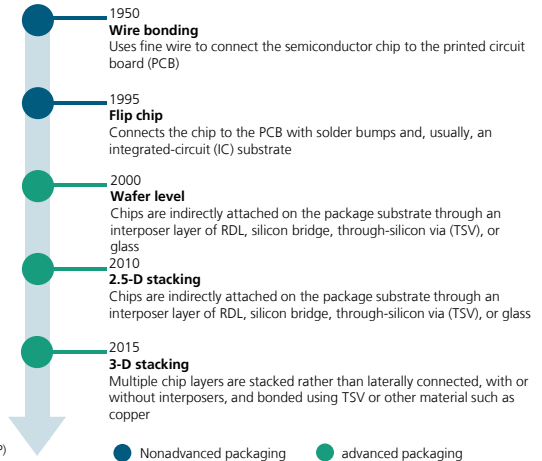
Interconnect technologies as the basis for AP

- The traditional workhorse of packaging, wire bonding, is coming to its limits
- Flip chip, contender to replace wire bond, sees shrinking contact dimensions (into the micron area), with substantial changes in technology (C4*, CuPillar, Thermocompression Bonding - TCB)
- Wafer scale packaging increases throughput of pre-fabricated system/module components tremendously, evolution pushing towards FO-WLP* and FO-PLP*
- Through Silicon Vias enable mass manufacturable IC stacking in 3D
- 2,5D integration using TSV and high density interposers become de-facto standard for Advanced Packaging paradigm
- Full 3D IC touted as ultimate goal of system integration

* controlled collapse chip carrier (C4), Fan out wafer level packaging (FO-WLP), panel level packaging (PLP)

Source: Burkacky, O., „Advanced Chip Packaging: How Manufacturers can play to win, May 2023, McKinsey Report

Timeline of packaging technology



Capability and Perspective Comparison of Packaging Technologies available at IZM



WireBond



FlipChip



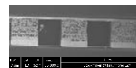
μFlipChip



μPillar FlipChip



Hybrid Bonding

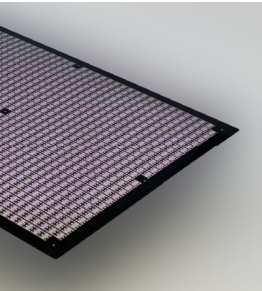


Polymer Hybrid Bonding

| | | | | | | |
|--|-----------------|----------------------------------|----------------------------------|----------------------------------|------------------|----------------------------------|
| Pitch (μm) | 30* | 100 | 20 | 5 | 0,2 | 1 |
| Interconnect Density (IO/mm ²) | 10 ¹ | 10 ¹ -10 ² | 10 ³ -10 ⁴ | 10 ⁴ -10 ⁵ | >10 ⁶ | 10 ⁵ -10 ⁶ |
| Interconnect process | sequentially | Parallel, Die | Parallel, Die | Parallel, Die | Parallel, Wafer | Parallel, Wafer |
| Infrastructure requirement | low | low | medium | high | Very high | high |
| Cost | low | low | medium | high | Very high | high |
| Future perspective | declining | stable | growing | Growing+ | Growing+ | growing |

* peripheral contacts, all others area array contacts

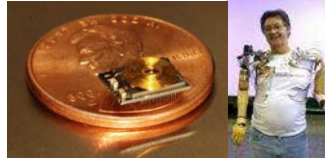
Highlights of the past decade, IZMs contribution to global innovation



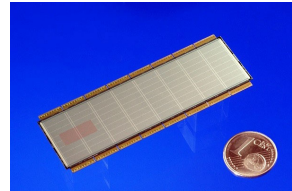
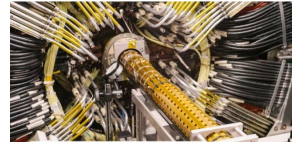
gration



Photon Counting Array
for CT Medical Scanner



Brain Computer Interface
(BCI) with wireless
transmission



Particle Counter for the
Higgs-Boson Experiment
at CERN

Technology for LED Matrix Wins the Deutscher Zukunftspreis

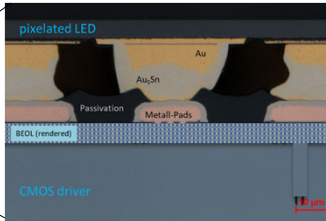
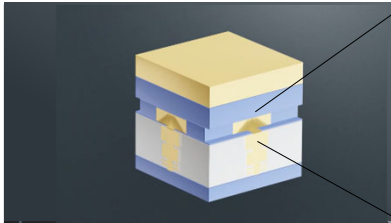
High-resolution light distribution and energy efficiency



DEUTSCHER ZUKUNFTSPREIS
Preis des Bundespräsidenten
für Technik und Innovation

Winner 2024

The Federal President's Award
for Innovation and Technology



Digital Light

- Car headlights illuminate the road ahead without endangering oncoming traffic or pedestrians
- 25,600 LEDs in a matrix of 320 x 80 points, where each individual LED can be controlled with a digital signal

Technology

- Gold-tin-solder is a robust and reliable interconnect, which has been proved even in space applications
- Fine pitch flip chip assembly chip-to-wafer was developed for high volume manufacturing and transferred

The Award

- The German President's Deutscher Zukunftspreis (German Presidents Prize for Future) is one of the most prestigious accolades for scientific achievement in Germany
- The team: Dr. Norwin von Malm, Stefan Grötsch (ams OSRAM) and Dr. Hermann Oppermann (Fraunhofer IZM)

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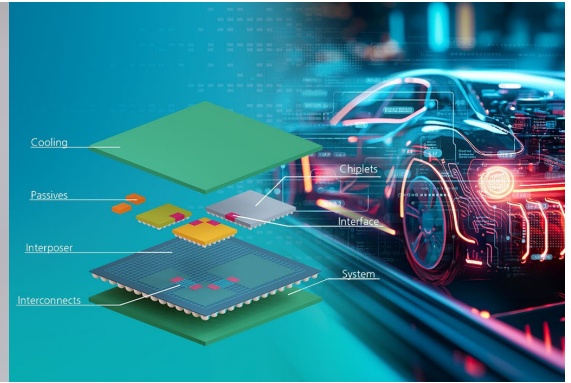
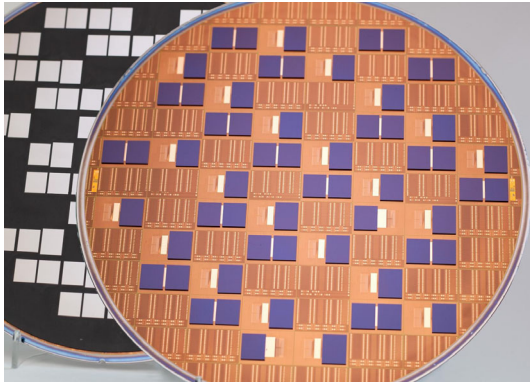
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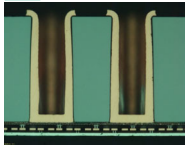
Environmental Impact of modern electronics (Hyperscaler AI)

Future Activities

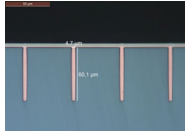
Chiplets – Integration on HD Interposer Wafer



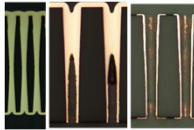
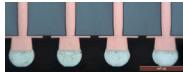
Innovations provided by IZM for Next Gen Devices: Through „X” Vias



▪ Post CMOS Blind Vias



▪ Interposer TSV
@ 300mm



▪ Through Glass Vias

▪ Multi Material Via Generation

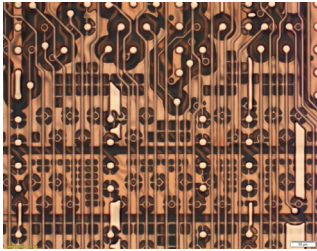
- Si
- SiC
- Glass
- Ceramic
- Polymer (PCB, EMC, Flex)

With high AR and smallest dimensions (down to 30nm!)



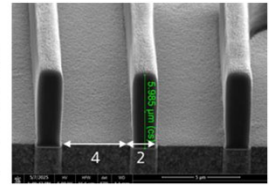
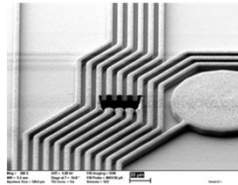
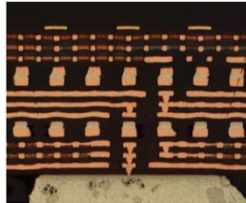
▪ Through SiC Vias

Innovations provided by IZM for Next Gen Devices: High Density Routing



▪ Si & Glass substrates:

- Sub μm Lines/Spaces to 200nm
- Micron scale TSVs with 20:1 AR



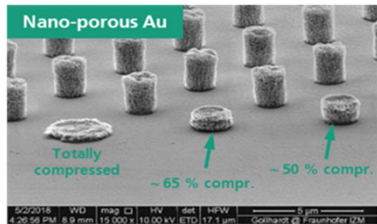
▪ Organic substrate

- $< 2 \mu\text{m}$ Lines/Spaces
- $< 10 \mu\text{m}$ TMVs with 20:1 AR

▪ Multi Layer (U)HD Interconnect Routing

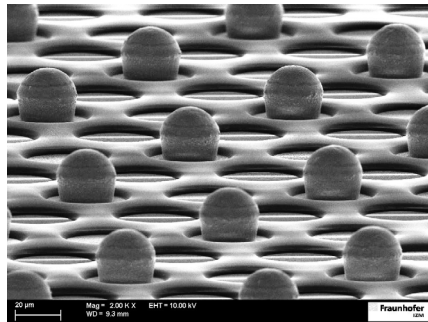
- Layer by Layer
- Tiled Layering

Innovations provided by IZM for Next Gen Devices: Chiplet Preparation



- Adaption of pad layout to bond process design for optimum DfM adoption
- Interconnect elements (μ -Bumps) for D2W and D2D integration

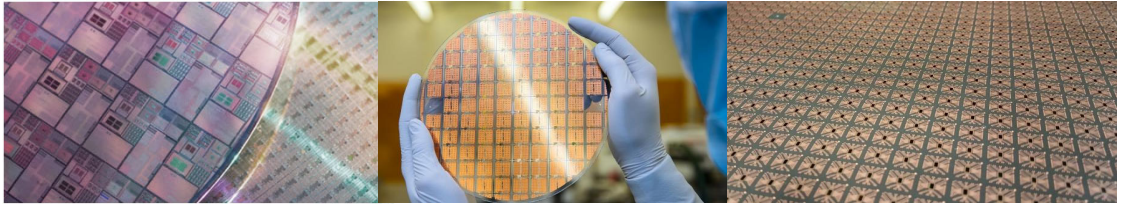
- Miniaturisation of μ Bumps towards 2 μ m bump dimensions
- Novel structures for integration (nano-sponges, xNT bumps)



Images: Forschungsfabrik Mikroelektronik Deutschland: IZM

Paradigm Change – Bringing together Wafer- and Panel-Level System Integration

IZM taking up the challenge – Pushing BEoL into the large area backend processes



CMOS Feature Sizes 5 nm ... >100 nm

WLP Feature Sizes 0.75 μm ... >10 μm

PLP Feature Sizes < 5 μm ... 100 μm

Wafer Level Packaging (WLP)

Based on thin film materials & equipment
100 mm ... up to 300 mm
CMOS – III/V - WBG wafers

2.5D / 3D integrated systems or system components

Technology
Format
Input
Output

Panel Level Packaging (PLP)

Based on PCB materials & equipment
up to 610 x 456 mm²
CMOS – III/V - WBG dies (w/ bumping)
Packaged / embedded modules

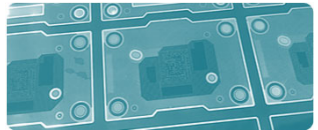
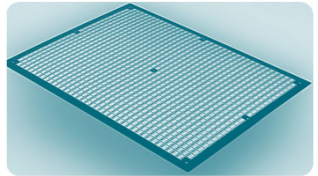
Next-Level Panel Level Packaging – IZM forming global consortia

High Volume demand of Large Area (Chiplet-) Packages and involvement of large industrial players indicate a next wave of Panel Level Packaging

With AI driven growing Package size, cost efficient Chiplet Packaging will rely on Panel Level Packaging technologies

At increasing I/O and decreasing L/S, technologies of high precision assembly, molding/embedding and fine RDL processes are requested

Digital Process Monitoring and Assembly Design Kits (ADKs) as part of the digitization are key to ensure fast evolving process flows



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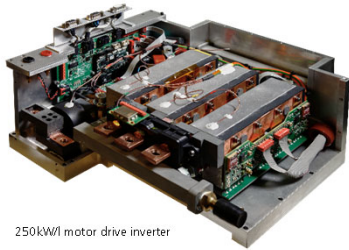
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Power Electronics – New Applications and New Devices Push Innovation Needs

IZM acting at the forefront of innovation

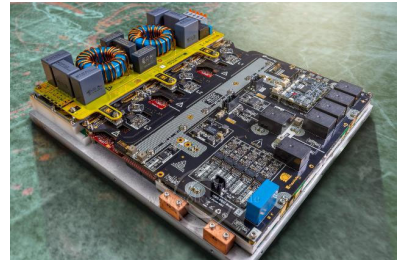
- The electrification of the world economy will increase demand for power electronics by an order of magnitude
- Less resources have to be used for it at higher efficiency
- High productions numbers require automated production



250kW motor drive inverter

IZMs solutions:

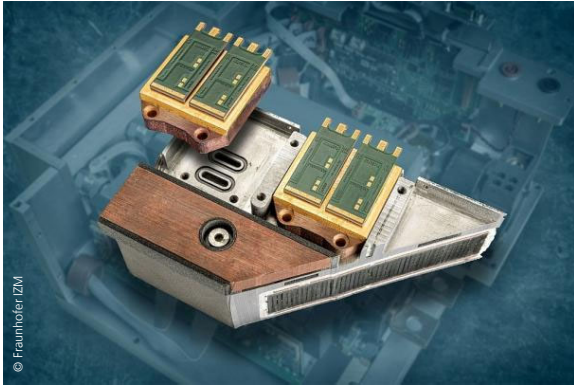
- Faster switching, smaller passives
- Circuit development adapted to production methods
- Deep engineering supported by computerized optimization



7kW OBC with flat magnetics

Novel Packaging Solutions for Highest Power Densities in MDI

Power Delivery & Thermal Management in **Motor Drive Inverters** suitable for high performance BEVs



- 48 embedded SiC ICs with minimum parasitics
- Power rating 600kW (peak 1000kW)
- System scale cooling using optimized 3D additive manufacturing of Cu cooling body in intimate contact with the ICs, offering a 10l/min coolant flow to limit ΔT to 20K
- Integration of modules directly onto Al-heat spreader
- No wirebonds, highly robust package

BMFTR project „DauerPower“, with Porsche AG & Robert Bosch GmbH

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Paradigm Shift in Data Centers

Packaging for Photonics → Photonics for Packaging

Bottleneck: Off - Chip/Chiplet/Core Interconnects

Next generation systems for all identified high performing applications / industries (where big-, secure-data is in) including System-in-Package and System-on-Chip, is the lack of off-chip/chiplet/core interconnects with

- low-latency,
- high-bandwidth,
- Low energy consumption
- and high density.

The requirement addressed by IZM - integration of the **photonic layer** within the 3D SiPs/SoCs towards a converged electro-optical system.

The photonics layer will be part of the interconnect layer.



Innovations for optical communication - addressing PICs, CPO & PhWB

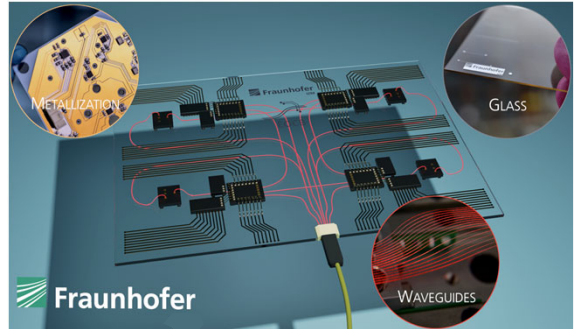
Glass as interposer for low loss light wave guides:

- Planar integration
- High precision structuring
- Compatible to electronic circuit boards

Platform for Photonic Integrated Circuit (PIC) assembly

Optimally suited for Co-Packaged Optics (CPO) concepts

Perfect match with Photonic Wirebonds (PhWB)



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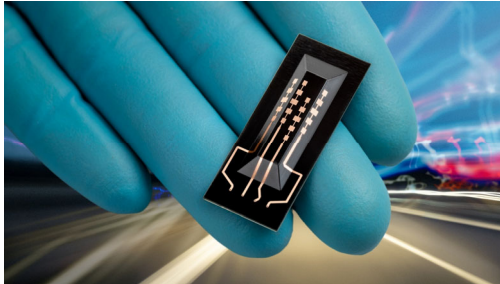
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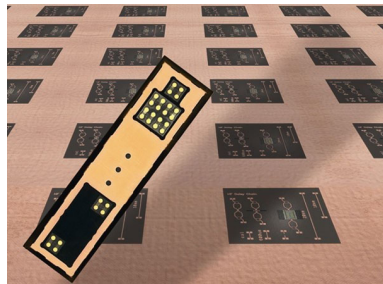
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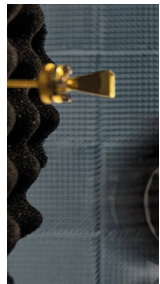
RF and High Speed Design – Technology Co-Optimization



3D Antenna with embedded RF-IC



77GHz Radar Module



Reflector

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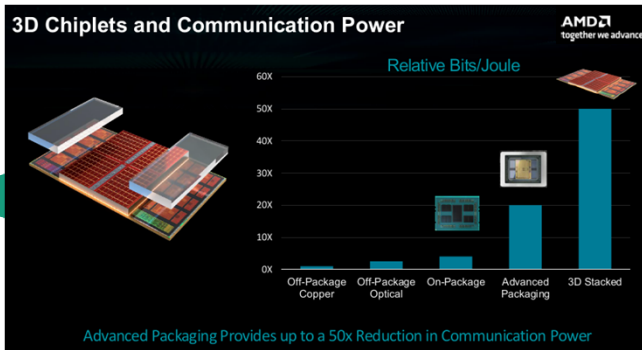
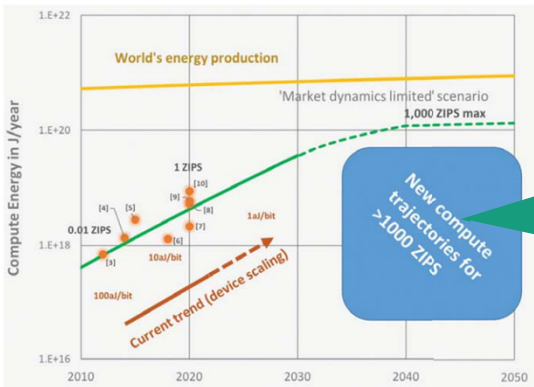
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Advanced Packaging to assist in tackling the challenge

IZM's technology capabilities trending, environmental assessment integral to IZM's DNA



Why the IT Giants Are on the Quest for Enhanced Environmental Transparency

Green Manufacturing – a trend IZM can support at any stage

Product Carbon Footprints for Semiconductor Devices need to be “actionable”

Short-term:

✓ **identify hot-spots / map emissions** (to develop GHG reduction strategy)

✓ **cooperate** with fabs on GHG reductions

✓ **coinvest** alongside suppliers to decarbonise activities

✓ **regulation**

✓ **tracking progress** of interventions

✓ **calculating scenarios, forecasts**

✓ **internal carbon prices**

Mid- to long-term:

✓ **supplier selection** (based on comparable PCFs)

✓ **inform chip design**



= mainly **supply chain management**, focussed on taking action, product carbon footprint as KPI, well beyond “reporting only”

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Packaging for Advanced Quantum Applications

Integration Technologies of Fraunhofer IZM as part of Germany's QNC initiative

1. Superconducting Interposer

- Redistribution layer (Nb and NbN),
- Superconducting TSVs

2. Cryo FlipChip

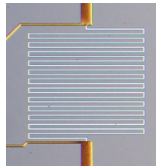
- Bumping indium and indium-tin less than 10 μm pitch
- Fine pitch flip chip bonding

3. Photonics: PIC Design & Integration Technology

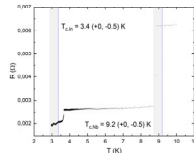
- Chip-to-chip optical coupling solution (butt, GC or evanescent)
- PIC integration technology to connect each qubit
 - Electrical routing on PIC wafer (RF multi-layer, TSVs)
 - Integrate mechanical stops to enhance placement accuracy

4. Cryogenic Test Capabilities

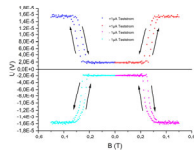
- Temperature ramp from 300K to 3.2 K,
- Magnetic field application up to 0.7 T
- RF capability up to 20 GHz



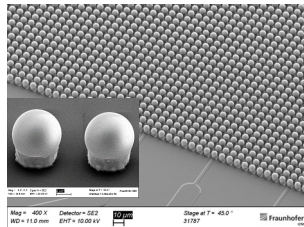
Patterned Nb lines



Test critical temperature



Test critical magnetic field



In bumps
7.5 μm pitch

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