Electronic Packaging Days 2025

Rolf Aschenbrenner

Enabling the Future – APECS Pilot Line

Strengthening Europe's technological leadership

Pilotlines in Pillar 1

Pillar 1

»Chips for Europe Initiative«
Strengthening research, development and innovation

NanoIC | FAMES greener electronics | APECS European Chiplet Innovation | WBG Wide Band Gap future power electronics | PIXEUROPE

Pillar 2

»Security of Supply«
Support for new types of production facilities and EU foundries

Pillar 3

»Monitoring and Crisis Response«
Coordination mechanism for monitoring the supply of semiconductors

APECS European Chiplet Innovation

KEY FACTS

- Total Budget: 730 Mio EUR
- Project duration: Q4/2024 – Q2/2029
- Consortium: 10 partners from 8 European countries

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Pan European Pilot Line Facility: Categorization of Pilot Lines

On Definition of RTO Pilot Line vs. Industrial Pilot Line

Leverage on increase of production capabilities

Transfer/Scale-up

RTOs Pilot Lines „Innovation Push“ – ‚Best in Class‘		Industrial Pilot Lines „Scale Up“
Exploratory Services (lower TRLs)	Small Scale Production (mid to high TRLs)	First Industrial Deployment (highest TRLs)
Delivery of Prototypes ▪ Basic architectures and feasibilities for products at an early stage (e.g. for proof-of-concept) ▪ Processes are far from final maturity ▪ PDK* drafted, initial models in place	**Delivery of small volume** ▪ Technology and Processes can already be used for prototypes and products ▪ Technology frozen, customer specific adaptations possible ▪ PDK* available ▪ Small scale production capacity available (industrial grade)	**First delivery of qualified Products** ▪ Technology, Processes and Production Methodology under evaluation ▪ Up-scaling of a R&D project ▪ Yield still to be improved, thus, no competitive production possible yet ▪ PDK* finalized

APECS delivers technologies, chips and solutions for next generations of applications in communication, sensing, power, quantum computing, etc.

RTOs Research

Industry Production

*** PDK**: process design kit, model of the fabrication process to be used for the **chip design**

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European Infrastructure

Pilotline for Advanced Packaging and Heterogeneous Integration for Electronic Components and Systems

P/ADK Design Flows

STCO Design

Interface Processing

Chiplet Integration

- Hetero-integration into (quasi-) monolithic integration
- Chiplet integration platform (2.5D and 3D)

Analysis & Metrology

Characterization, Test & Reliability

Application Solution developed under the EU Green Deal

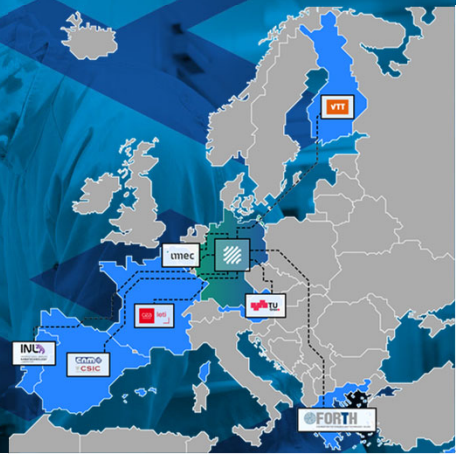
Users

- SMEs
- Start-ups
- System / Design Houses
- IDMs
- RTOs
- Universities

Overall budget
730m
app 500m CAPEX
app 230m OPEX

Duration
12/24 - 12/29

Funding
EU 50%
BMFTR 33%
Federal states 17%



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Chiplet Integration Platform

Chiplet Interface Readiness for Heterogeneous Integration

Chiplets from external partners (RTOs, IDMs, Foundries,…)

Compute and Memory Integration

MEMS Integration

Photonics Integration
InP Tx Chiplets
GaN/GaAs Laser

RF Integration
InP-on-BiCMOS
Chiplet BiCMOS-CMOS
GaN-on-SiC HEMT /
InGaAs-on-Si HEMT

Characterization Test Reliability

Chiplet Integration Platforms

Functional Interposer

RF/Photonic/MEMS Interposer
200 mm Si/Glas

Ultra High Density Interposer
300 mm Si

Reticle Size Limitation

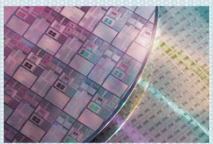
Glass as an HD Option

Organic/Glass Interposer
Up to 600 mm

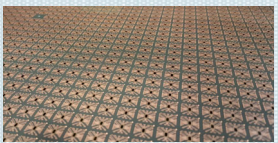
Second Level Assembly

Toolbox for Functional Integration and Advanced Packaging
3D Stacks, Si-Bridge, µ-Bumps, Embedding, Assembly, Package-on-Package, …..

Wafer Level Packaging (WLP)



Panel Level Packaging (PLP)



APECS Demonstrators

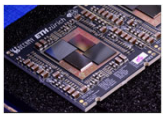
Demonstrator HPC

Demonstrator MEMS

Demonstrator Photonic

Demonstrator RF

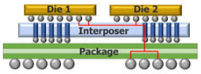
Characterization Test Reliability



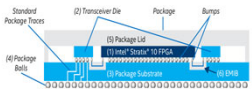
Functional integration, miniaturization, flexibility, scalability

2.5D Packaging Technologies

Silicon

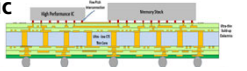


Silicon Interposer [1]

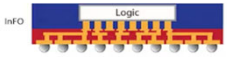


Silicon Bridge [2]

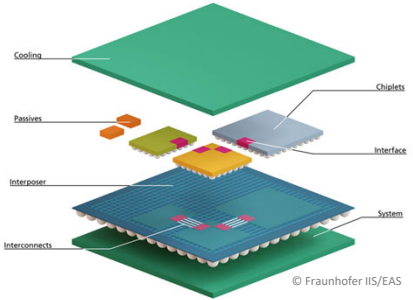
Organic



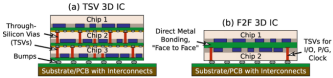
Organic Interposer [3]



Fan-out wafer-level packaging (FOWLP)[4]



3D Packaging Technologies



3D Stacked Die [5]

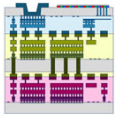


Image Sensor [6]

Chiplet system

Performance	Cost	Reliability
Product responsibility	?	Supply Chain
Safety & Security	Testability	Software

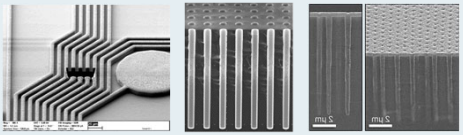
1 Siemens EDA, from "Dissolving The Barriers In Multi-Substrate 3D-IC Assembly Design" blog Semiconductor Engineering, Feb. 22.
2 Intel, https://semiengineering.com/using-silicon-bridges-in-packages/ July 20, 2018
3 Electronic Components and Technology Conference 2015, Modeling, design and fabrication of ultra-thin and low CTE organic interposers at 40µm I/O pitch
4 TSMC, Siemens: https://resources.sw.siemens.com/en-US/white-paper-implementing-fan-out-wafer-level-packaging-fowlp-with-the-hdap-flow
5 Heterogeneous 2.5D and 3D Integration for Securing Hardware and Data | SpringerLink
6 Arizona State University

Chiplet Integration Platform

Functional Interposer

Target

- Anorganic Interposers for advanced CMOS on 300mm
- Multi-Functional Interposers for RF, Optoelectronics & MEMS*
- Passive Functionalities in Interposer
- Organic HD Interposers
- **Providing all required technologies for interposers based chiplet integration**



Innovations

- Sub-micron TSV´s, AR20:1,UHD Routing – incl. PostCMOS
- Glass, HR-Si, Ceramics with TxV´s and resp. routing, on 200mm
- IPDs, integrated cooling, LWGs, structural features
- Advanced HD substrates (5µm L/S)
- Laminates with embedded IC
- Panel Scale Interposers using FO processes

Impact

- Preparation for UHD Wafer Scale Integration, supporting QMI and Advanced Packaging
- Interposers serving Multi-Domain Systems (MEMS, Opto, RF, Sensing, *) for broad range of functionalities
- Critical functionalities integrated in a single process flow
- Module- and System Interfaces towards the applications

** Power Electronics is served but was excluded from the text due to potential interference with the PowerSemiconductor Pilot Line*

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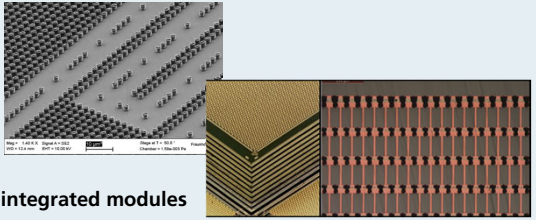
Chiplet Integration Platform

Functional Integration

Target

- 3D Stacking of advanced CMOS wafers and non-CMOS heterogenous/multimaterial wafers
- 2.5D Integration of chiplets onto interposer
- Preparation for chiplet interfaces
- Specific technologies for MEMS and sensor chiplets
- **Providing all technologies to realize heterogeneously integrated modules**



Innovations

- High density Wafer2Wafer stacking with sub µm precision using hybrid bonding
- Stack-integration of specific functionalities for HIS providing hermeticity, capping
- Die2Wafer integration for heterogenous functionalities
- Chiplet interface adaption with RDLs, terminal metal & bumps

Impact

- Chiplet based module realization with functionalities from different domains
- Highest density integration of heterogenous chiplets
- Enabling STCO methodology throughout domains

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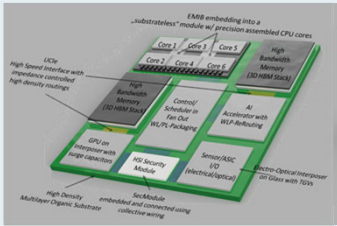
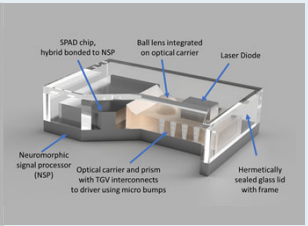
Chiplet Integration Platform

Advanced Packaging & Assembly

Target

- System scale assembly for Heterosystems with Modules and Subsystems
- Quality and Reliability assured functionalities at system level
- Novel integration concepts for 3D volumetric systems

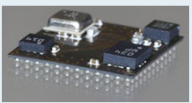




Innovations

- High density, high speed, assembly on advanced substrates
- Reliable assembly for multi-layered heterogenous systems (L1-L3)
- Embedded and fan out integration of systems
- Hybrid integration concept using embedding and fan out on panel scale
- Layer-by-Layer stacking for 3D volumetric system integration

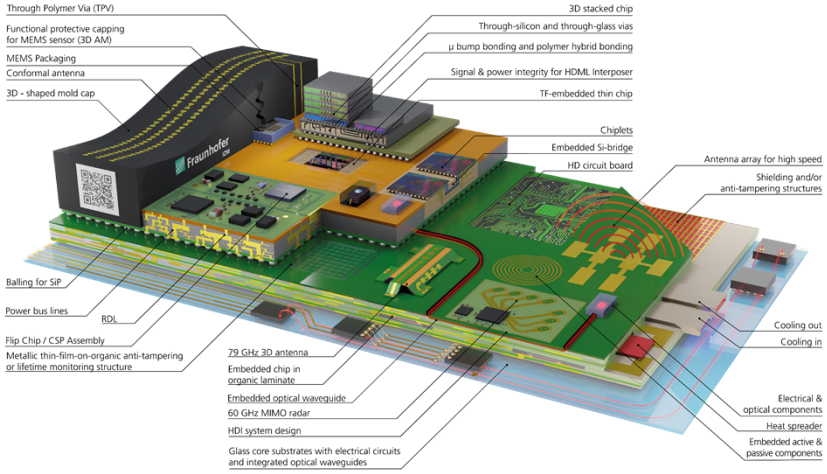
Impact



- Functional highly integrated systems for novel applications like AI, autonomous mobility, RF and Communication, Sensors, Power and Photonics
- Supporting STCO methodology from L1-L3

Hetero-Integration Technologies and Advanced Packaging

Bringing microelectronics into application



Coordinated by

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Implemented by

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Pilot Line Project Partners

Fraunhofer MIKROELEKTRONIK

FBH Ferdinand Braun Institut

ihp

TU Graz

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cea leti

FORTH

CNM CSIC

INL International Iberian Nanotechnology Laboratory

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SACHSEN-ANHALT

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ANR Agence Nationale de la Recherche

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Flanders State of the Art

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