Fraunhofer IZM

Fraunhofer Institute for Reliability and Microintegration IZM

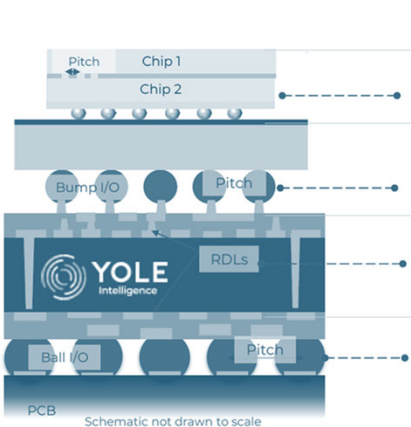
Electronic Packaging Days 2025

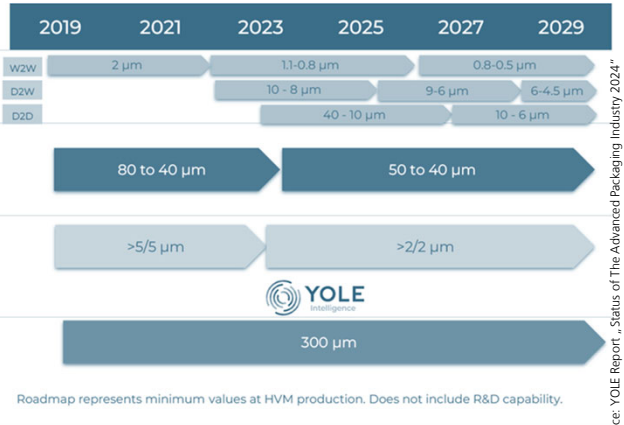
Dr. Manuela Junghähnel

Navigating the Future: Innovation and Roadmapping in Wafer Level Packaging

Advanced packaging roadmap: I/O pitch and RDL L/S

A typical flip-chip IC Substrate





Bump I/O pitch is scaling much faster than Ball I/O pitch which drives a finer RDL L/S at IC substrate package level.

Source: YOLE Report „Status of The Advanced Packaging Industry 2024"

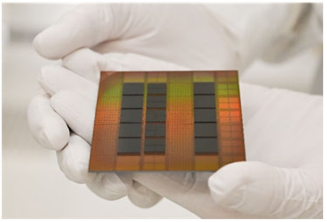
Semiconductor packaging technology is the key pillar if the future is digital

Goals

- the continued reduction of interconnection pitch - enabled by TSVs, TMVs, microbumps, and more aggressively, hybrid bonding.
- Further shrinking via diameter and wafer thickness.

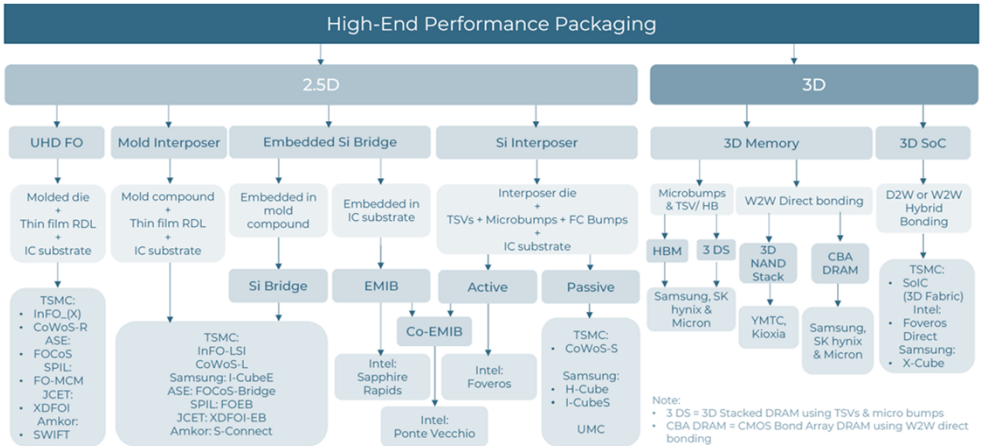
Driver Technologies

- Hybrid bonding for 3D SoCs.
- Chiplet-based and heterogeneous architectures
- Co-Packaged Optics
- Glass is gaining momentum as a core substrate material
- Toward 3.5D Packaging: converging toward platforms that combine 2.5D and 3D integration



Photos: Sylvia Wolf

Advanced packaging roadmap: Technologies for 2.5 and 3D integration



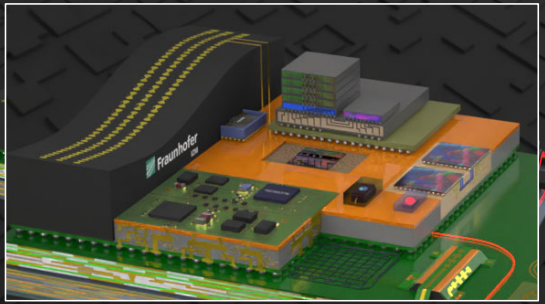
Source: YOLE Report „High-End Performance Packaging 2025 | Report | www.yolegroup.com"

The APECS pilot line – European chiplet innovation

Advanced **P**ackaging and Heterogeneous Integration for **E**lectronic **C**omponents and **S**ystems

Heterogenous integration on wafer-level

- 3D processing
- TSV, TGV
- Embedded Si bridge
- UHD Si Interposer
- Cu/Cu hybrid bonds
- µPillar + C4 Bumping



- Integrated Cooling
- Embedded Passives
- Signal integrity
- Power delivery
- FI- / FO-WLP
- Mix-Pitch assembly

APECS

Co-funded by the European Union
Bundesministerium für Forschung, Technologie und Raumfahrt
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Freistaat SACHSEN
Fraunhofer IZM

Fraunhofer IZM – Wafer Level Integration

Infrastructure & Process Capabilities

ISO 9001-certified process lines at two locations (Berlin & Dresden) for process development, material and equipment evaluation as well as R&D and industrial services on automated and semi-automated production equipment

WLSI Berlin:

Vast variety of materials, processes and wafer materials / sizes suited for R&D prototyping and small volume manufacturing, TRL 2 – 9

ASSID Dresden:

Industry-compatible process line for 200 / 300mm Si and glass wafers and prototyping for small to medium volume manufacturing, TRL 6 – 9

Berlin

ISO 9001 2015 CERTIFIED

Dresden

Fraunhofer IZM (Berlin)

1000 m² clean room area (ISO 4-6)
Wafer sizes: 100, 150, 200 mm (partially 300 mm)

Fraunhofer IZM-ASSID (Dresden)

900 m² clean room area (ISO 6-7)
Wafer sizes: 200 mm + 300 mm

APECS

Fraunhofer IZM

WLSI Research Infrastructure Berlin

100-200mm clean room (expanding 300mm capabilities)

Process line for advanced prototyping and pilot manufacturing

- 2.5D / 3D integration (SiP, CSP) for a variety of semiconductor materials
- Polymer/Cu-based high density multilayer RDL
- Silicon interposer with application specific TSV integration (via middle, via last, back side TSV) and Glass interposer with TGV, both with high density, multi-layer RDL
- Advanced interconnect solutions for photonics, RF and MEMS packaging and power (Cu/Sn(Ag), Cu/Sn, Ni/Au, sulf. or cyan. Au, AuSn, NPG, In, InSn)
- Temporary/Permanent wafer bonding (adhesive, solder, anodic, direct)
- High accuracy flip-chip assembly (D2D, D2W)
- Fan-In and Fan-Out wafer level packaging (high density RDL first/last, multi chip (Si, GaAs, GaN, SiC, …))
- High energy particle, x-ray and IR detector module flip-chip interconnects and assembly
- Wafer-level MEMS packaging and prototyping of MEMS sensors
- Development of photonic systems (design, hybrid EIC/PIC integration, characterization)

ISO 9001:2015 certified | MES

Wafer Processing and Assembly Clean Room
1000 m²
ISO 3 – ISO 5

100–200mm process line for 2.5D/3D heterogeneous wafer level system integration (expanding 300mm capabilities)

Capacity for several 100 wafers per year with TRL 2 – 9

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ASSID Research Infrastructure Dresden

200/300mm clean room

Process line adjusted to development, prototyping and low volume manufacturing under industrial manufacturing conditions.

- 3D wafer-level SiP, CSP
- Application-specific Cu-TSV integration: via middle, via last, backside
- Si interposer with TSV, multi-layer RDL, micro-cavities, integrated passives
- Glass interposer w/wo TGV, multi-layer RDL and µ-interconnects
- High-density, multi-pitch & size micro-bump or pillar interconnects (Cu, SnAg, Au, Ni)
- Pre-assembly: thinning, thin wafer handling, laser & mechanical singulation
- 3D assembly: D2D, D2W, W2W, 3D WL stacking
- Temporary/permanent wafer bonding (adhesive, soldering, direct)
- Direct bond interconnects (DBI) – W2W, D2W
- High density multi-layer polymer RDL for advanced high density flex, flex/silicon & RDL-1st FOWLP applications

ISO 9001:2015 certified | MES

R&D clean room ASSID1: 800m² ISO-class 6, lab space: 300 m² ISO-class 7

Leading edge process line for 2.5D/3D heterogeneous wafer level system integration equipment compatible to run 200mm/300mm wafer-FOUP

Capacity for several 100-1000 wafers per year with TRL 6 – 9

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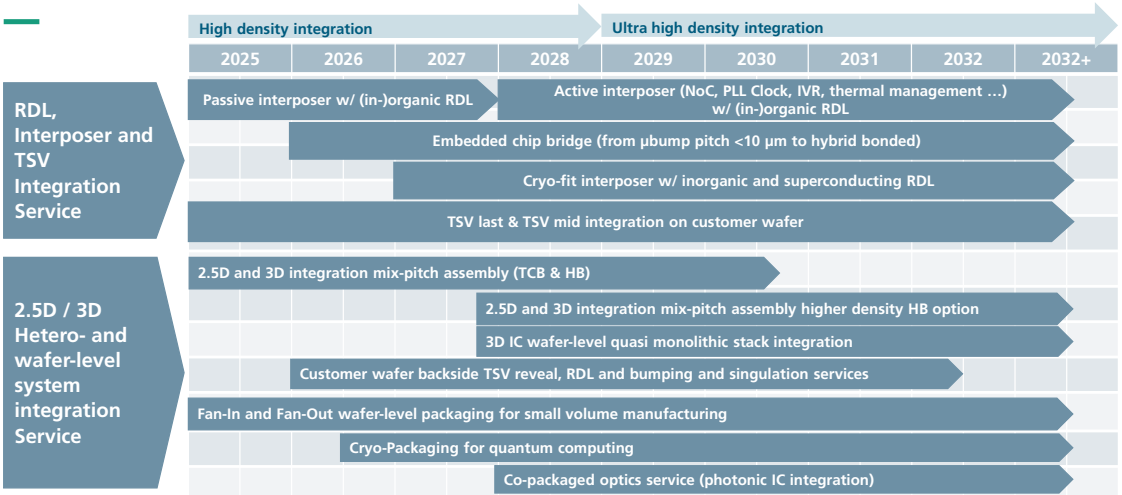
Technology Roadmap: 300 mm 2.5 und 3D Wafer Integration Technologies



PLL Clock – phase locked loop clock
IVR – Integrated voltage regulator
NoC – Network on Chip

RDL – Re-Distribution Layer
TSV – Through Silicon Via

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APECS Pilot Line - What we offer on Wafer Level?

Technologies & Services

- From design to packaging & characterization
- 2.5D/3D integration up to 300 mm, fan-in /-out wafer-level packaging, UHD interposer, hybrid bonding, micro-bumping
- Access to design kits (PDK/ADK), advanced prototyping & pilot production

Chiplets & Components

- Design and manufacturing of chiplets for client use
- Combining CMOS, RF, MEMS, photonics, sensors, and more
- Versatile platform supporting chiplets from multiple sources with standard and custom interfaces like UCIe and BoW

Demonstrators

Four demonstrators show a seamless process chain:

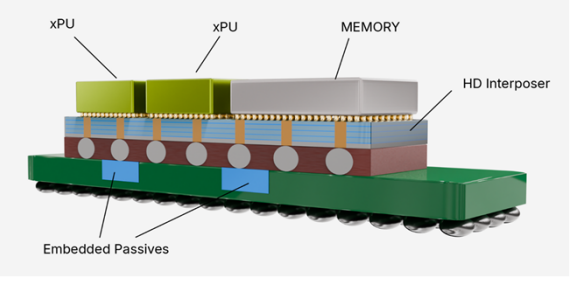
- **HPC:** High-performance computing module with hybrid chiplet integration
- **Sensor:** Multi-material sensor system with heterogeneous & QMI integration
- **Photonics:** High-speed photonic module with InP-EML arrays & photonic wire bonding
- **RF:** RF module up to 300 GHz, integrating InP, GaN, SiGe, BiCMOS & advanced packaging

APECS Pilot Line - What we offer on Wafer Level?

Demonstrator Example: High Performance Computing (WP 6.1)

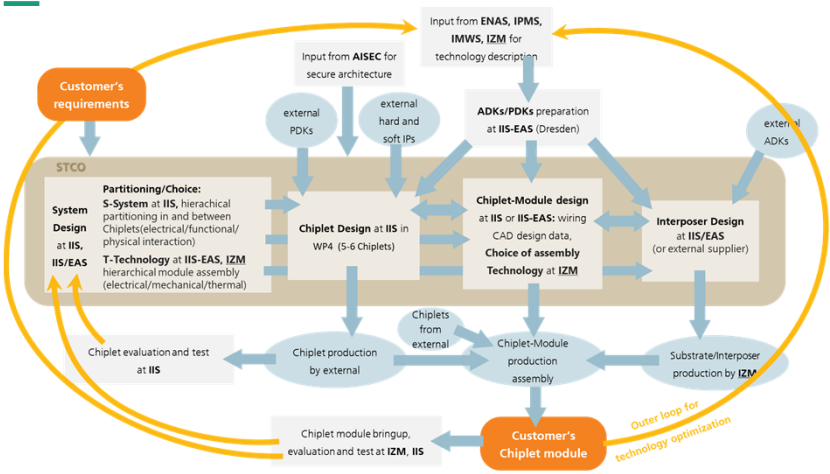
Lead: Fraunhofer IIS and IZM-ASSID

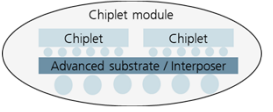
- STCO concepts will be enabled and used for a first-time right functionality from the design to manufacturing and verification measurements comparing simulations with the results.
- The institutes IIS & AISEC are involved for chiplet architecture specification, fabrication and test and packaging development and interposer and assembly developments.
- IZM, IZM-ASSID, IPMS and IIS, IIS-EAS, AISEC focus on the overall targets for system architecture, STCO and chiplet/interposer interface.
- A security analysis will be carried out by AISEC. The chiplets to be integrated in this demonstrator are designed in WP4 (STCO design).

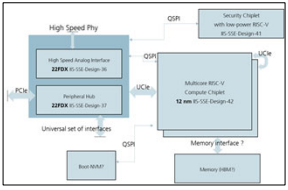


APECS Pilot Line - What we offer on Wafer Level?

Demonstrator Example: High Performance Computing (WP 6.1)





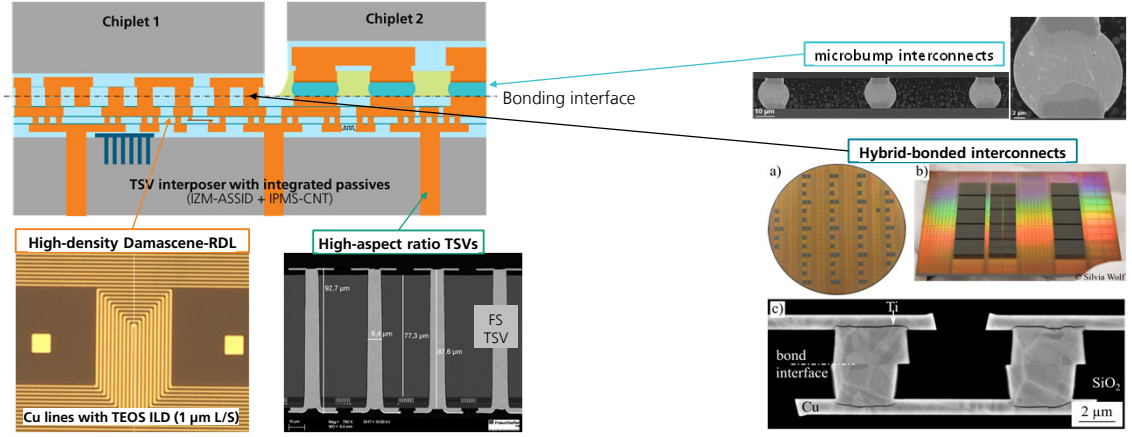


Topology of the HPC demonstrator

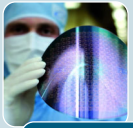
APECS Pilot Line - What we offer on Wafer Level?

Demonstrator Example: High Performance Computing

Heterogeneous mixed-pitch chiplet integration for ultrahigh I/O densities



IZM Research and Development Services on Wafer Level provided to Industry



Feasibility Studies

Demonstrators

Prototypes

Pre-Series

Pilot Fabrication

Low Volume Manufacturing

IZM joyn APECS pilot-line of FMD

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Thank you for your attention

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Contacts for Wafer Level System Integration

Dr. Michael Schiffer
Head of Department
Wafer Level System Integration Berlin (WLSI-B)

Phone: +49 30 46403-234
E-Mail: michael.schiffer@izm.fraunhofer.de

Fraunhofer IZM
Gustav-Meyer-Allee 25
13355 Berlin
www.izm.fraunhofer.de

Dr. Manuela Junghähnel
Head of Department
Wafer Level System Integration Dresden (WLSI-DD)
All Silicon System Integration Dresden - ASSID

Phone: +49 351 795572-18
E-Mail: manuela.junghaehnel@assid.izm.fraunhofer.de

Fraunhofer IZM-ASSID
Ringstrasse 12
01468 Moritzburg
www.izm.fraunhofer.de