Fraunhofer IZM

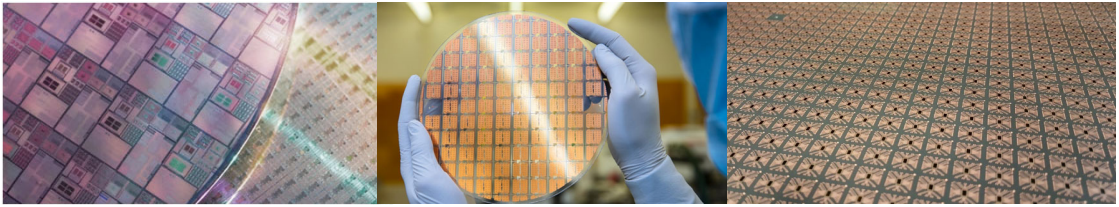
Fraunhofer Institute for Reliability and Microintegration IZM

Electronic Packaging Days 2025

Ruben Kahle

Next-Level Panel Level Packaging

From Wafer- to Panel-Level System Integration



CMOS Feature Sizes 5 nm … >100 nm | WLP Feature Sizes 0.75 µm … >10 µm | PLP Feature Sizes < **5 µm … 100 µm**

	Wafer Level Packaging (WLP)		**Panel Level Packaging (PLP)**
	Based on thin film materials & equipment	**Technology**	Based on large area processes, materials & equipment
	100 mm … up to 300 mm	**Format**	up to 610 x 456 mm² | 510 x 515 mm²
	CMOS – III/V - WBG wafers	**Input**	CMOS - III/V - WBG dies (w/ bumping)
	2.5D / 3D integrated systems or system components	**Output**	Packaged / embedded modules

Next-Level Panel Level Packaging

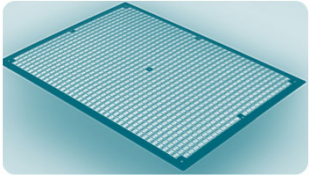
Overview

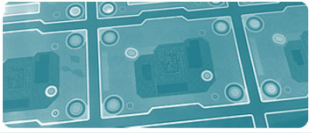
High Volume demand of Large Area (Chiplet-) Packages and involvement of large industrial players indicate a next wave of Panel Level Packaging

With AI driven growing Package size, cost efficient Chiplet Packaging will rely on Panel Level Packaging technologies

At increasing I/O and decreasing L/S, technologies of high precision assembly, molding/embedding and fine RDL processes are requested

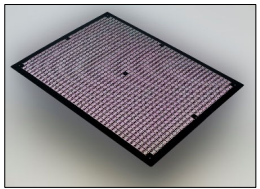
Digital Process Monitoring and Assembly Design Kits (ADKs) as part of the digitization are key to ensure fast evolving process flows



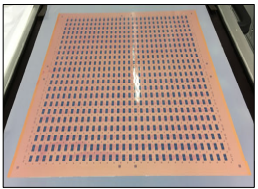


Next-Level Panel Level Packaging

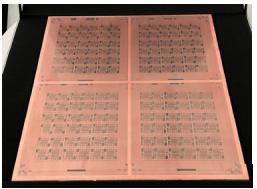
Examples of Large Scale Panel Architectures at Fraunhofer IZM (610 x 457 mm² | 515 x 510 mm²)



Epoxy Mold Compound



Organic / Prepreg



Glass

DIE FIRST

FOPLP

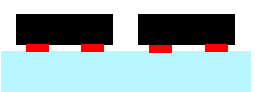
Embedded Substrate

Embedded Glas Core

RDL FIRST

PLP

IC Substrate



Glas Core Substrate

Next-Level Panel Level Packaging

Integrated R&D Line | Status and Outlook with APECS

Cleanroom

Clean / Condition

- RENA Spray
- Glass Cleaning Line

Coat / Dev.

Spin/Spray tool

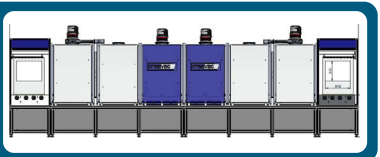
Vac Lam.

Dynachem

PAB/PEB

Hot Plate

PVD metal deposition



Creamet 600 CL3S4

DI Image

- Direct Imaging 1 µm
- Schmoll MDI Ultra 2µm

RDL Plate

LAM Kallisto

ICP Etch

ICP Etch

CCP Etch

RIE Evatec

CMP

CMP

Test/Inspect

- ATG A9+
- KLA UD900

supported by APECS

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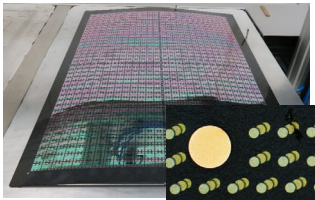
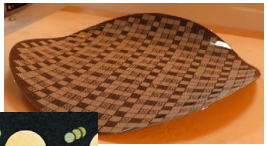
Fan Out Panel Level Packaging

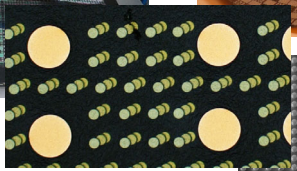
Fan Out Panel Level Packaging

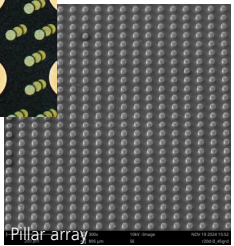
Research Topics | Overview

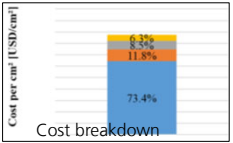
- **Warpage**
- **Die Shift / RDL shift**
- **Ultra-fine line RDL**
- **Multi-layer molding**
- **Cost / environmental Modeling**











Cost breakdown

Fan Out Panel Level Packaging

Research Topics | Focus 1: In-Situ Sensor Data of Compression Mold Process

Sensor Mold Tool:

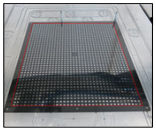
- Tool mounted, time synchronized sensors on 8 positions
- Pressure, temperature and cure conversion of EMC during process
- Optional carrier mounted strain sensor for cure shrinkage

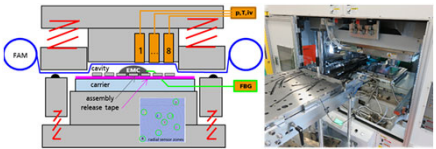
Cavity Sensors:

- Temperature (T) → real T at cavity / FAM interface to EMC
- Pressure (p) → location dependent evolution of p
- Ion viscosity → cure status by dielectric analysis (DEA)

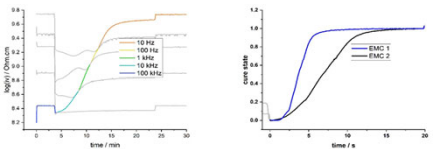
to enable Condition-Monitoring & Digital Process Analysis

Molded FO-Panel





Sensormoldtool



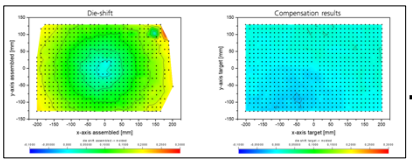
Inmold Cureverlauf

Fan Out Panel Level Packaging

Research Topics | Focus 2: Die Shift Challenge

Solving the Die Shift Challenge:

- During Setup Phase: determination of die shift factors (Data driven compensation algorithms)
- Compensation of the rough die shift by adapting the placement positions using the die shift factor
- Compensation of fine die shift by adapting the panel design using the die shift factor



Step A – minimize deviations post encapsulation

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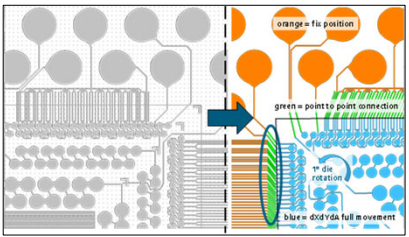
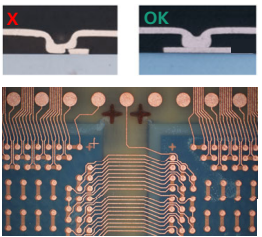


Step B – adapt layout to align shifted components

=

matching RDL and Die



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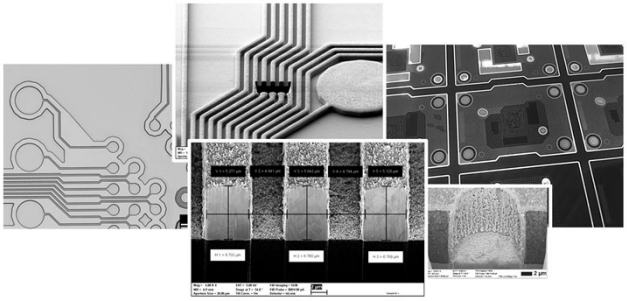
Organic / IC Substrates

Organic Substrates

Research Topics | Overview

- **Next-Gen Organic Cores (CTE, E-Modulus)**
- **Component / Die Embedding**
- **RDL with Photodielectrics / Plasma Vias**
- **Hybrid approaches SAP / Damascene (CMP)**
- **Fine Pitch Bumping (Cu Pillar)**



Organic Substrates

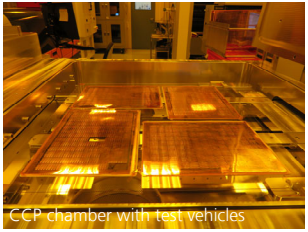
Research Topics | Focus 1: RDL formation with Plasma Etching and Ashing

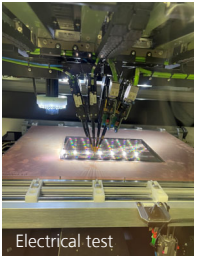
Plasma Etching (CCP):

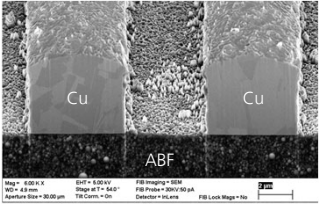
- Reactive etching of Titanitium
- Backsputtering of Cu
- Etching into Highly filled dielectrics w. Soft/Hard mask
- Descum of PIDs

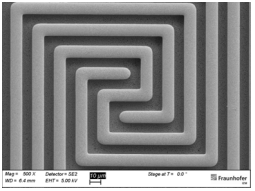
Plasma Ashing (ICP):

- Resist Residues
- Resist in volume
- Surface Cleaning


CCP chamber with test vehicles


Electrical test





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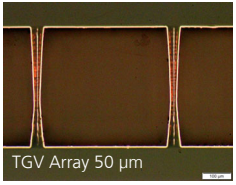
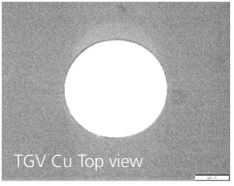
Glass Core Substrates

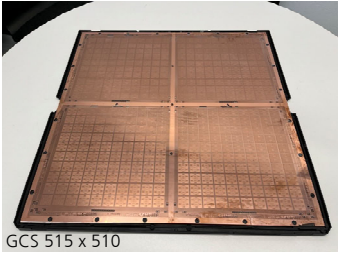
Glass Substrates

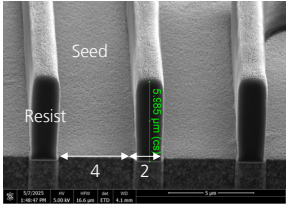
Research Topics

- **Panel Handling & System Reliability**
- **Through Glass Via (TGV), & Glass cavity**
- **Glass Trim & protective Coating**
- **Embedded components**
- **Multilayer Fine Line RDL**
- **Photonics integration**









Glass Substrates

Research Topics | Focus 1: TGV manufacturing and Cu fill

TGV Formation:

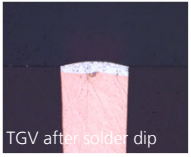
- Glass modification and Etching
- Analysis Methods

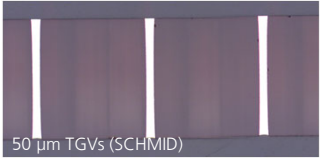
TGV Cu-Fill:

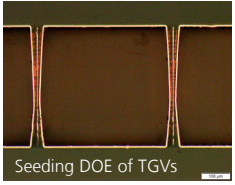
- Buffer / Linker / Brush layer application
- Seeding & Plating

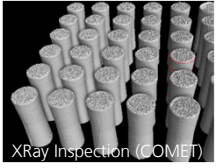
Reliability & Analysis:

- Thermal Shock & Cycling
- Electrical test
- Cross sections, SEM / FIB


TGV after solder dip


50 µm TGVs (SCHMID)


Seeding DOE of TGVs


XRay Inspection (COMET)

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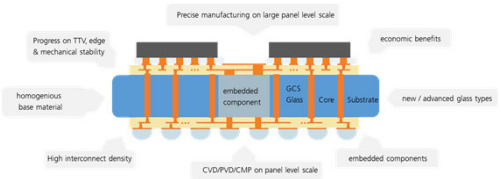
How To Collaborate?

Glass Panel Technology Group

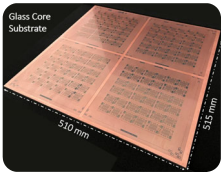
Project overview

GLASS PANEL TECHNOLOGY GROUP

Kick-Off Meeting Oct 2025



Long Term Vision



GCS 510 x 515mm²

GCS building Blocks	Project Plan Year 1	Y2	Y3 ++
TGV	TGV > 50µm | t = 700µm | AR < 1:10	TGV ≤ 50µm | t > 700µm | AR > 1:15	TGV ≤ 50µm | t > 500µm | AR > 1:20
	TGV BKM and R&D: laser modification, etching, coating, metal seeding (plasma, wet), plating, CMP, etching, AOI ++		
RDL	SAP 5µm L/S, Via 15µm, ABF	SAP 2µm L/S, Via 10µm, PID	SAP 2µm L/S, Via 5µm, PID
	RDL Photo dielectrics on panel scale; RDL damascene approaches; RDL Buffer / intermediate layer on glass		
	Panel construction / Handling; Glass Trim & Coating; Component assembly;		

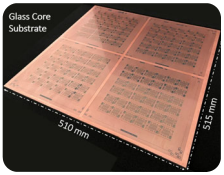
Glass Panel Technology Group

Project overview

GLASS PANEL TECHNOLOGY GROUP

Kick-Off Meeting Oct 2025

Partner Companies



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Thank You

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