How To Use The APECS Pilot Line
– Strategic Partnership and Service Offer -

APECS: Advanced Packaging and Heterogeneous Integration for Electronic Components and Systems

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Purpose of the APECS pilot line

- Position **Europe´s R&D and industry at the forefront of semiconductor innovation**
- Establish a **cutting-edge infrastructure** for heterogeneous integration and chiplet technology
- Advance **technological capabilities for cutting-edge semiconductor devices**
- **Support European industries** (e.g., automotive, telecom, healthcare, IoT)
- Lead the way in **advanced packaging and heterogeneous integration** by providing diverse technologies on a single platform

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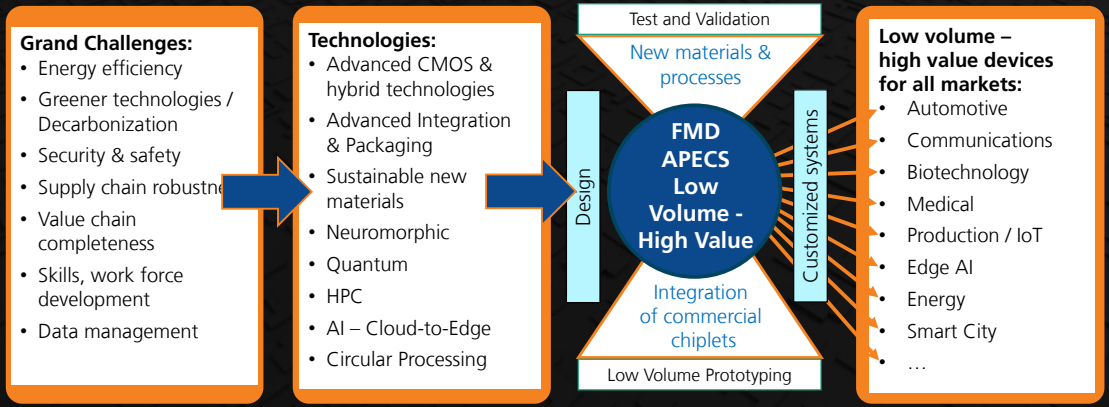
EU Chips Act: Contribution of FMD

FMD: Advanced Packaging and Heterogeneous Integration for Electronic Components and Systems



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FMD joins forces with Europes´ leading RTOs

VTT: IPD and RF on silicon and glass substrates; Heterogenous 3D integration: ALD for TSV and Wafer Level and LTCC Packaging of RF and optical MEMS

imec: RDL 1st Chiplet Packaging Demonstrator and Chiplet Integration Package

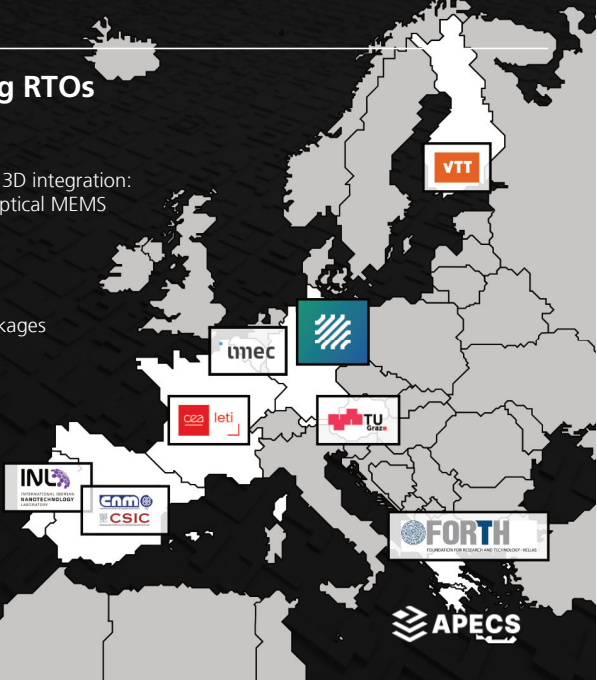
CEA-Leti: FOWLP technology for RF (>150GHz) System-in-Packages (SiP) and Glass substrates for > 100GHz RF passive component

TU Graz: ESD for heterogeneous integration

INL: 3D heterogenous integration of graphene FET biosensors

CNM/CSIC: Microchannel cooling, Printed antennas

FORTH: 3D Sequential Integration (3D SI) of GaN based RF front end (RFFE) chips



What are the challenges in heterogeneous integration?

Design complexity

- Integrating different materials (CMOS, InP, GaAs, SiPh)
- Managing electrical and optical coupling
- Ensuring co-design efficiency and thermal stability

Standardization

- Defining universal design rules
- Standardizing interfaces
- Ensuring process compatibility
- Establishing reliability benchmarks

Manufacturing precision

- High density interposers (organic/inorganic)
- Sub-micron alignment
- Controlling process variations
- Enabling stress-free bonding
- New testing concepts

Cost management

- Reducing fabrication costs
- Improving yield
- Scaling automated assembly
- Minimizing supplier dependency

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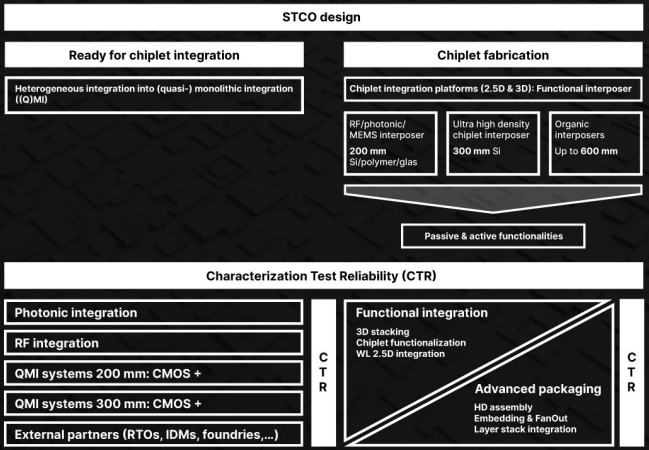
APECS brings the connection between design, technology and testing for wide range of applications



All the developments are taking place under the dictum of the European Green Deal.

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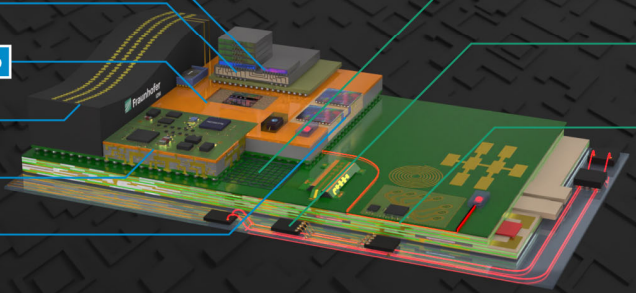
Examples for the integration at wafer and substrate level

Integration at wafer level

- Hybrid Cu/Cu bonds
- HDML Si-Interposer
- TF-embedded thin chip
- 3D-shaped mold cap
- TSV/TGV/TPV
- Embedded Si-bridge



Integration at substrate level

- Metallic TF-on-organic anti-tampering structures
- Embedded passives, chips or SiP module
- Embedded optical waveguides

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Key innovations of the APECS pilot line

1. Worldwide first **advanced automotive chiplet integration platform** (2.5D and 3D) for multiple core technologies (CMOS, Opto/RF) and non-electronic devices (MEMS, Opto, OLED), leveraging the innovations of advanced packaging

2. **Comprehensive end-to-end design flow and methodology** for chiplet-based advanced heterogeneous systems integration – Design-for-Performance, -Yield, -Power Efficiency, -Testability

3. Expansion of hetero-integration into **quasi-monolithic integration (QMI) for highest performance density** by leveraging Back-End-of-Line and Advanced Packaging capabilities

4. Prototyping of **high performance chiplet-based systems for specific needs of the European industries**, in particular, automotive, medical device and health care, sensors and advanced manufacturing industries

5. **Novel backend-of-line interfacing technology** for MEMS, opto/RF chips (III/V RF chiplets with (Bi)CMOS for 300 GHz+ frequencies)

6. **Novel testing concepts and technologies** for function-, quality- and yield- optimization

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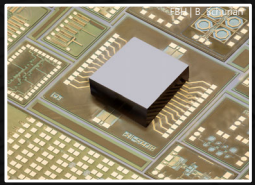
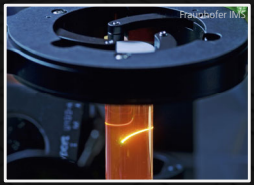
Application areas of the APECS pilot line

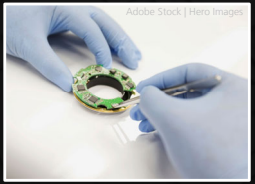


High performance computing



Sensor systems

Industrial manufacturing



Medical instrumentation

Telecommunications

AI/ Machine Learning

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Potential for industrial uptake

Users

- Chip Foundries
- Integrated Device Manufacturer (IDMs)
- Materials & Tools Supplier
- Semiconductor Customer
- Research Community
- Start-ups

Value Proposition

Design Services: enable chip, chiplet IP, and system design for APECS Pilot Line; provide and operate design platforms with support

Process development, materials and tool validation: accelerate technology development and validate processes for commercial transfer

System Development: leverage APECS tech for new products and business; enable access to specialized technologies

Manufacturing Outsourcing: offer Proof of Concept, prototype runs, small-volume production, and scalable transfer options

Research Access: support research-to-application transfer; Provide easy access via local competence centers

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What we offer

Category	Example services
Surface technologies	PVD, CVD, LPCVD, ALD, CMP, …
Packaging & Assembly	Direct wafer bonding, C2W, TSVs, nano TSV, Flip chip, …
Inline measurment	In-line SEM, Overlay, Elipsometry, 3D surface metrology, …
CTR	RF characterization, CDM test system, Plasma-FIB SEM defect screening, …
Chiplets & Sensors	SiGe BiCMOS-InP-DHBT, InP EML chips, photo detectors, gas sensors, …
Design	PDK/ADK offers (interposer & chiplet integration, design platform)

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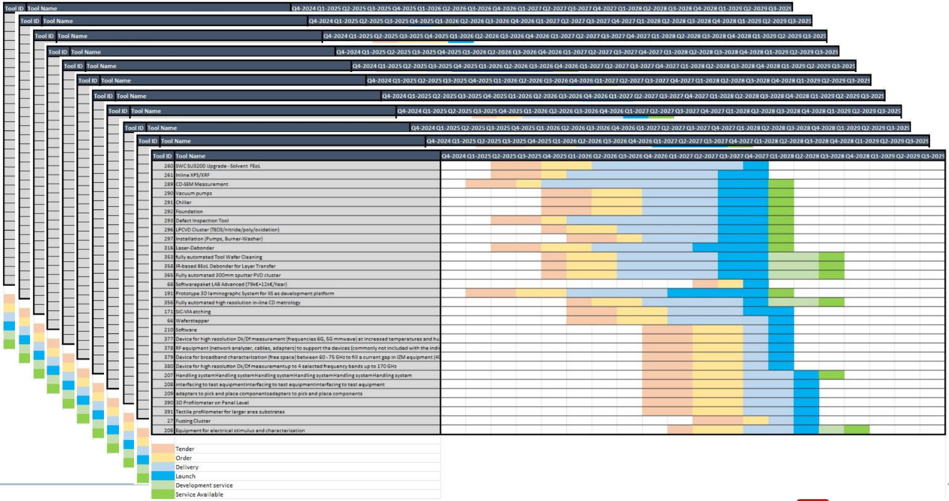
Coordination of service provisioning

Collection and clustering of services in APECS



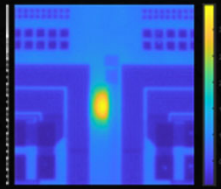
Coordination of service provisioning

Collection and clustering of services in APECS

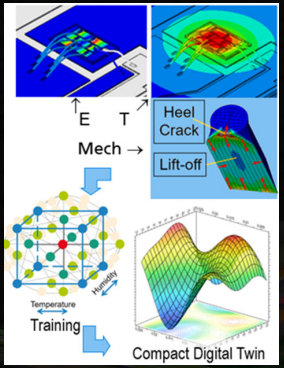
Service list – example (full)

Which device/tool/tool category is used	Name of the R&D service	Description of service (2-3 sentences/bullets)	Technical details for pot. clients	Cluster	When is the service avail
Process step / module	CVD	BTBAS Oxide / Nitride deposition on 8" wafer	only valid for cmos compatible 8" wafer fabrication	Suface Technologies	Q3/2026
Process step / module	Al-2-Al wafer bonding			Packaging and Assembly Technologies	
Technology	6" Interposer	MPW run with 4 levels of Al-interconnect layers with MIM and Thin-film-resistor module;	2 thin Al layers (500nm) and 2 top-metal layers with 2um and 3um	Packaging and Assembly Technology	Q3/2026
Technology	SiGe-BiCMOS-InP-DHBT	Chiplet integrated InP_DHBT on SiGe-BiCMOS	platform offer with PDK; accessible via MPW service(?)	Chiplets, Sensors, MPW	Q4/2028
Test & Metrollogy	Broadband Spectroscopy and thin layer characterization	8" wafer measurement in a cmos-compatible process environment		Characterization	Q3/2028
Design Service	PDK/ADK offer (Interposer & Chiplet Integration)			Design Others	Q3/2028
Process step / module	CMP	Polishing of oxide materials (e.g. SixOy, AlOx), nitride materials (e.g. TiN, SiXNH, metal si	only valid for cmos compatible 8" wafer fabrication	Suface Technologies	Q2/2027
Process step / module	CMP	Tungsten CMP	only valid for cmos compatible 8" wafer fabrication	Suface Technologies	available
Process step / module	PVD deposition	Oxide deposition (Ti2OS, SixOy, AlOx, ITO, AZO), Metal deposition (Ti, Al, TiW), Silicon d	only valid for cmos compatible 8" wafer fabrication	Suface Technologies	Q2/2027
Process step / module	PVD deposition	Deposition of Ti, TiN, TiW, W, AlSi, AlCu	only valid for cmos and MEMS 8" wafer fabrication	Suface Technologies	available
Process step / module	CVD deposition	Deposition of USG, Si	only valid for cmos and MEMS 8" wafer fabrication	Suface Technologies	available
Process step / module	Lithography	0,35µm resolution	only valid for cmos and MEMS 8" wafer fabrication	Suface Technologies	available
Process step / module	Oven processes	Annealing, wet/dry oxidation, TEOS, LPCVD SiN	only valid for cmos compatible 8" wafer fabrication	Suface Technologies	available
Process step / module	ALD deposition	Deposition of Al2O3, Ta2O5, TiO2, HfO2, ZrO2, AZO, TiN, Ru, 2D-Materials	available for cmos and MEMS 8" wafer fabrication as well as for ch	Suface Technologies	available
Process step / module	Dry etching	Etching of Si, oxide, DRIE, Poly, metalls	available for cmos and MEMS 8" wafer fabrication	Suface Technologies	available
Process step / module	Wet etching	HF, Caro-SC1, HSPOH, HNA, EKC, Scrubber	available for cmos 8" wafer fabrication	Suface Technologies	available
Process step / module	isotropic gas etching	HF_XF2	available for cmos and MEMS 8" wafer fabrication	Suface Technologies	available
Process step / module	Inline measurements	Ellipsometry, optical inspection, in-line SEM, XRD, Stress, Resistivity, Overlay, profiler, p	available for cmos and MEMS 8" wafer fabrication	In-line Measurements	available
Process step / module	Grinden / Dicing	Grinden, dicing cut, dicing	available for cmos and MEMS 8" wafer fabrication	Suface Technologies	available
Process step / module	Bonding	Direct Wafer bonding, C2W bonding	available for cmos and MEMS 8" wafer fabrication	Packaging and Assembly Technology	available
Process step / module	SEM	Cross section / FTIR	available for all Si devices	Reliability and Offline Measurements	available
Technology	Pressure sensor	capacitive and piezoresistive	demonstrator available	Chiplets, Sensors, MPW	available
Technology	PICs platform	combination of different photonic devices	demonstrator available	Chiplets, Sensors, MPW	available
Technology	IR-Detectors	micro-bolometer for different wavelengths	demonstrator available	Chiplets, Sensors, MPW	available
Technology	SPADs		demonstrator available	Chiplets, Sensors, MPW	available
Technology	Bio-/Gas-Sensors	CNTs, bio-functionalized surfaces	demonstrator available	Chiplets, Sensors, MPW	available
Technology	Acceleration Sensors	freqs standing MEMS structures	demonstrator available	Chiplets, Sensors, MPW	available
Technology	TSVs	Etching TSVs, ALD for TSVs and Cu-Plating	available for cmos and MEMS 8" wafer fabrication	Packaging and Assembly Technology	available
Device	InP-DHL Chips		Dedicated O- and C-band EML wafer runs on InP substrates	Chiplets, Sensors, MPW	Q3/2025
Technology	MPW Platform	InP MPW run on substrates	Photonic integrated circuit platform offer with PDK; accessible via	Chiplets, Sensors, MPW	Q1/2025
Technology	MPW Platform	LNOI MPW run on substrates	Photonic integrated circuit platform offer with PDK; accessible via	Chiplets, Sensors, MPW	Q3/2026
Device	High-Speed InP Photodetectors		Dedicated SVR photodetector wafer runs on InP substrates	Chiplets, Sensors, MPW	Q1/2025
Device	MPW Platform	MPW runs of MMICs based on GaN/SiCHEMT technology, CPW and MSL	platform offer with PDK; accessible via MPW service	Chiplets, Sensors, MPW	available
Device	MPW Platform	MPW runs of MMICs based on InGaAs-mHEMT and InGaAs-on-SiHEMT technologies;	platform offer with PDK; accessible via MPW service	Chiplets, Sensors, MPW	available
epitaxy	100 mm Epitaxial wafers	MOCVD grown GaN-based heterostructures	AlGaN/GaN heterostructures on s.i. SiC substrates	Suface Technologies	available
Device	Chiplet integration Platform	Heterointegration of GaAs laser chiplets on SiN passive photonic platform	Wavelengths: 630 nm - 1180 nm, Transfer printing + integration	Chiplets, Sensors, MPW	Q3/2029
Device	Chiplet integration based on InP DHBTs with BiCMOS	MOV runs dedicate for Chiplet integration of InP HBTs on BiCMOS		Chiplets, Sensors, MPW	Q3/2029
Process step / module	Blade dicing	Blade dicing for wafers of different materials (Si, glass, ceramic, etc.) including edge trim	200mm/300mm wafers as well as rectangular shapes; manufactur	Packaging and Assembly Technology	available
Process step / module	Die-to-wafer Bonding	Direct and hybrid bonding for chips to wafer	+/-300nm Platziergenauigkeit, 200mm/300mm Wafer, incl. Plasm	Packaging and Assembly Technology	Q4/2027
Process step / module	Pick & Place	Die sorting	200mm gross wafer packs, GelPak,	Packaging and Assembly Technology	available
Process step / module	Die-Bonding	Adhesive chip assembly	Dispensing, stamping of adhesives followed by chip assembly (+/-	Packaging and Assembly Technology	available
Process module	CMOS processing	Poly-Si-Gate with and without Nitrid-Spacer	200 mm wafers, 350nm process module	Chiplets, Sensors, MPW	available
Process module	CMOS processing	LOCOS isolation process	200 mm wafers, 350nm process module	Suface Technologies	available
Process module	CMOS processing	Salicide process: self-aligned Silicon Silicide for contact formation	200 mm wafers	Suface Technologies	available
Process module	CMOS processing	formation of contact holes	200 mm wafers	Packaging and Assembly Technology	available
Process module	CMOS processing	Planarisation, height differences of chiplets	200 mm wafers	Suface Technologies	Q3/2026
Process module	CMOS processing	BEOL metalisation	200 mm wafers, AlCu	Suface Technologies	Q3/2026
Process step / module	Lithography exposure	DUV for 130 nm fin, i-Line for 400 nm fin, Double-side Mask Aligner	only valid for CMOS and MEMS 6" wafer fabrication	Suface Technologies	available
Process step / module	Lithography coating	i-Line for 400 nm fin, double-side alignment	only valid for CMOS and MEMS 6" wafer fabrication	Suface Technologies	Q1/2027
Process step / module	Lithography coating	Spin, spray coating and development	only valid for CMOS and MEMS 6" wafer fabrication	Suface Technologies	available
Process step / module	PVD deposition	Evaporation of Al, SiO2, TiO2	only valid for CMOS and MEMS 6" wafer fabrication	Suface Technologies	available
Process step / module	PVD deposition	Spurter deposition of Al, AlSiCu, Ti, TiN, Ta, Ta2O5, Nb, Nb2O5, TiAl, Al alloys, Al2O3	only valid for CMOS and MEMS 6" wafer fabrication	Suface Technologies	available

Service Offer: Characterization, Test and Reliability



Electrical Fault Isolation



Novel testing concepts and technologies
for function-, quality- and yield- optimization

- **Comprehensive characterization, test and reliability platform** to support manufacturing
- Provision of complete **functional and reliability test** capabilities and strategies along the whole value chain
- Innovative and **unique test system** (photonics test head)
- **Test service** (volume test)
- **Knowledge transfer** (test hardware and methods)
- Support by **cutting-edge failure analysis** capabilities for industrial technology ramp up, series production and market introduction
- Support of continuous market success by field by **counterfeit detection and identification of IP violations**

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How to access APECS technologies

Submit your inquiry through our APECS website

Our access team evaluates your inquiry

Initial meeting to discuss your project

Access team involves technology experts to identify the most suitable FMD institute(s) for your project

Detailled discussion with institute(s) on project scope and contract conditions

Project implementation

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Kontakt

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