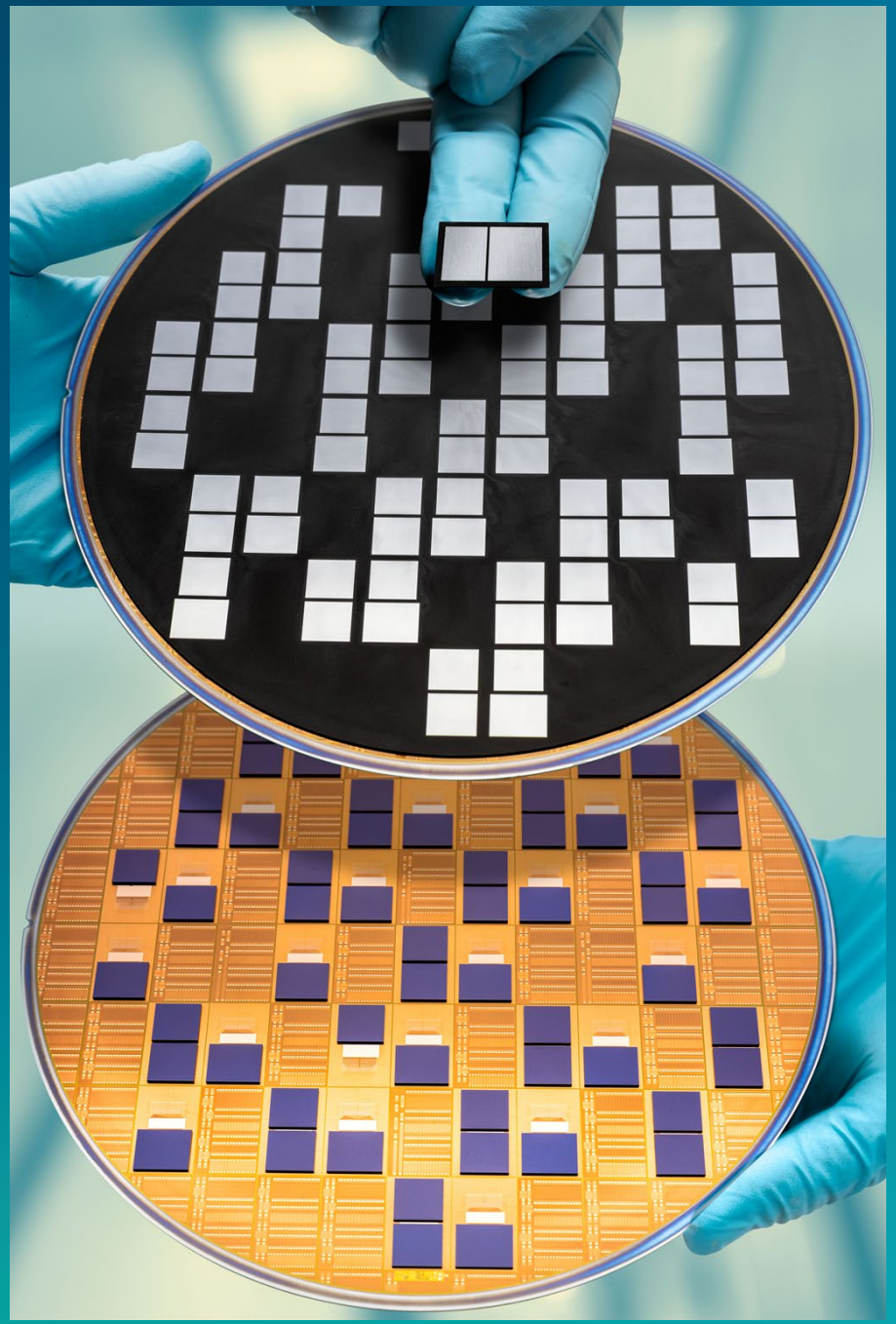


Fraunhofer IZM

Fraunhofer Institute for Reliability and Microintegration IZM

Electronic Packaging Days 2025

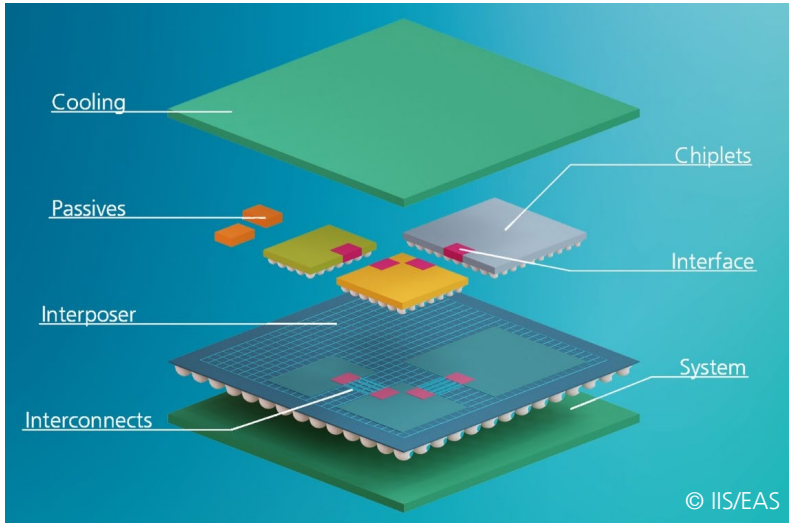
Keynote

Function-Driven Innovation: How Technology Follows the Needs of Chiplet Systems

Dr. Michael Schiffer
Head of Department WLSI

Content

- Chiplet Systems: Holistic Architectural System Strategy
- Architecture Customization by STCO
- Trends: From Substrate to Bridge Embedding to Interposer
- Project Highlights
- Key Messages



Vision of Chiplet Systems!

[…] It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected.
The availability of large functions, combined with functional design and construction, should allow the manufacturer of large systems to design and construct a considerable variety of equipment both rapidly and economically. […]

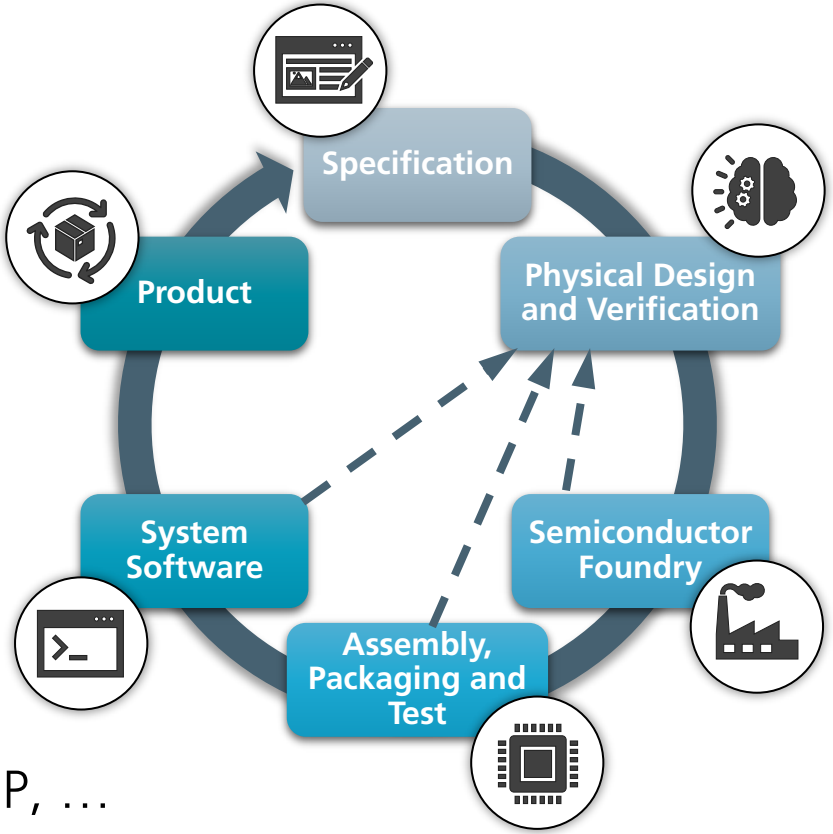
Gordon E. Moore, 1965

Chiplet Systems: Holistic Architectural System Strategy

Benefits and Challenges

Benefits:

- ***Cost Effectiveness:*** Higher yield and re-usability
- ***Scalability and Flexibility:*** Modularity and Node mix & match
- ***Faster Innovation:*** Parallelized chiplet development
- ***Performance:*** Application-specific design and technology

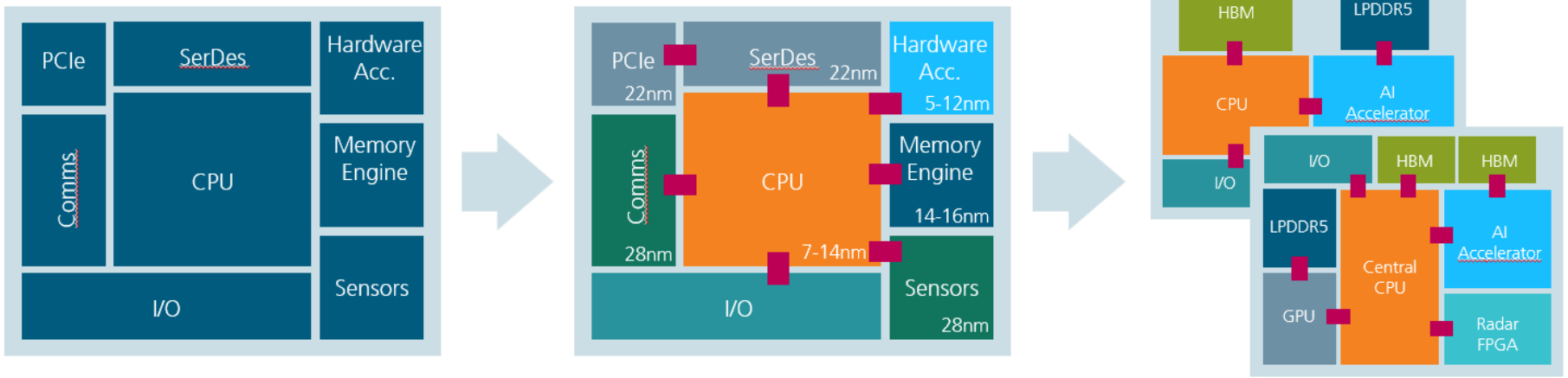


Challenges:

- ***Increased Design Complexity:*** Design beyond chip-outline
- ***Inter-Chiplet Communication:*** Standards definition, protocols, IP, …
- ***Packaging Cost, Yield and Physical Limits:*** Area-optimized system architecture, high yield on chiplet-level but probably lower yield on high-end package level (test strategy ?)
- ***Limited Ecosystem and Standards:*** Availability of re-usable chiplets and communication standards

Chiplet Systems: Holistic Architectural System Strategy

Chiplet System Architecture



Monolithic SoC Architecture

- Most advanced IP determines node complexity and cost
- Area limitation by wafer yield and stepper field

Chiplet System Architecture

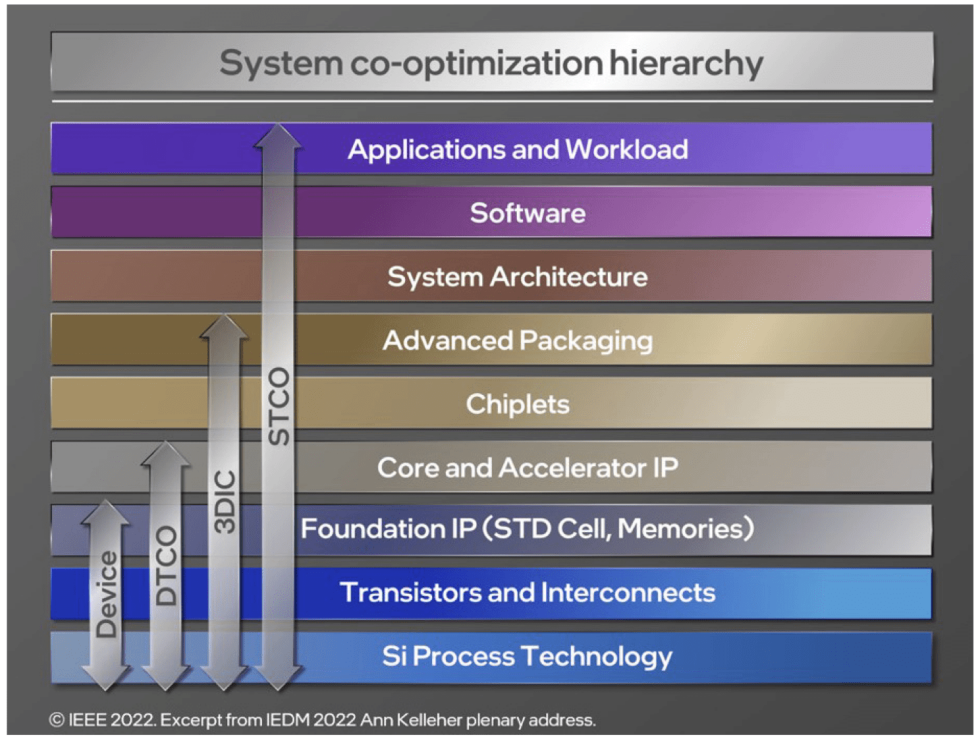
- Optimal usage of node and cost
- Area limitation by package yield
- Test strategy and bring up

Application-Specific Chiplet System Architecture

- Optimal usage of node and cost
- Area limitation by package yield
- Test strategy and bring up
- Optimal architecture for application

Architecture Customization by STCO

- ***Comprehensive approach to system design:*** System perspective in terms of signal and power integrity, thermal induced stress integrity → optimization of performance per area
- ***Reduction of cost and time to market:*** Highest quality level at shortest amount of time
- ***DTCO*** leads to better profit for lithography, wafer processing, testing and yield, while as ***STCO*** leads to best choices in chiplet and routing arrangement, technology selection and system-level testing
- ***DoE short loops*** with in-line characterization to feed-back critical information for physical design



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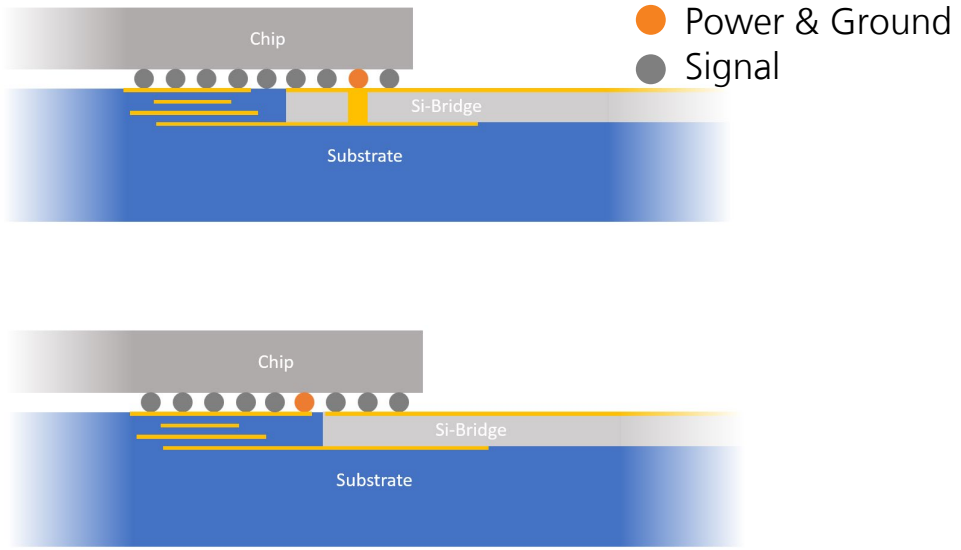

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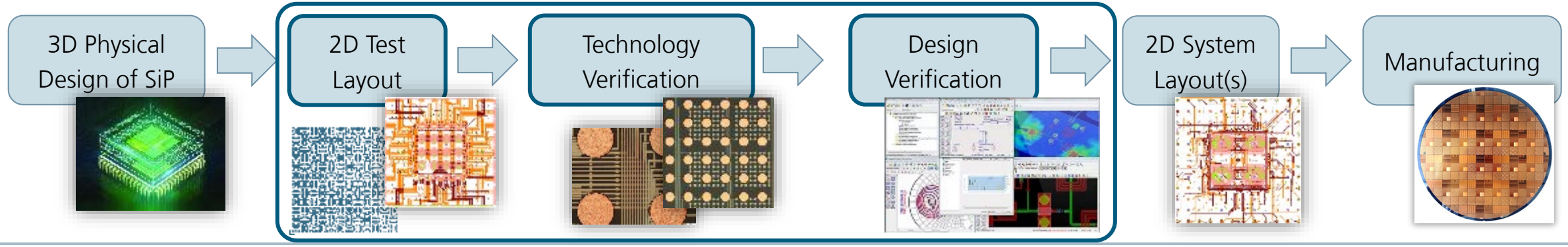

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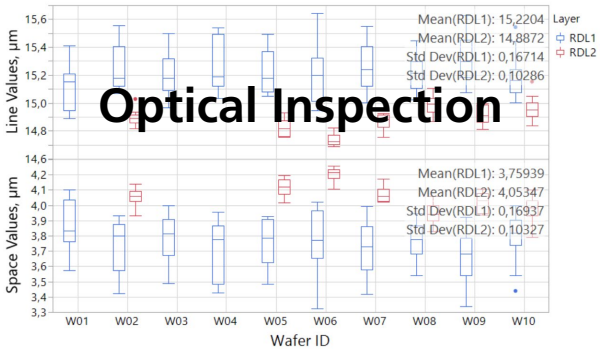
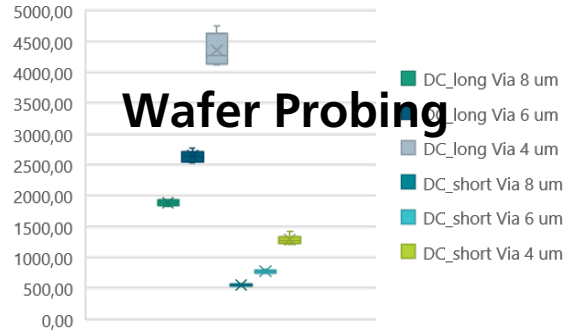
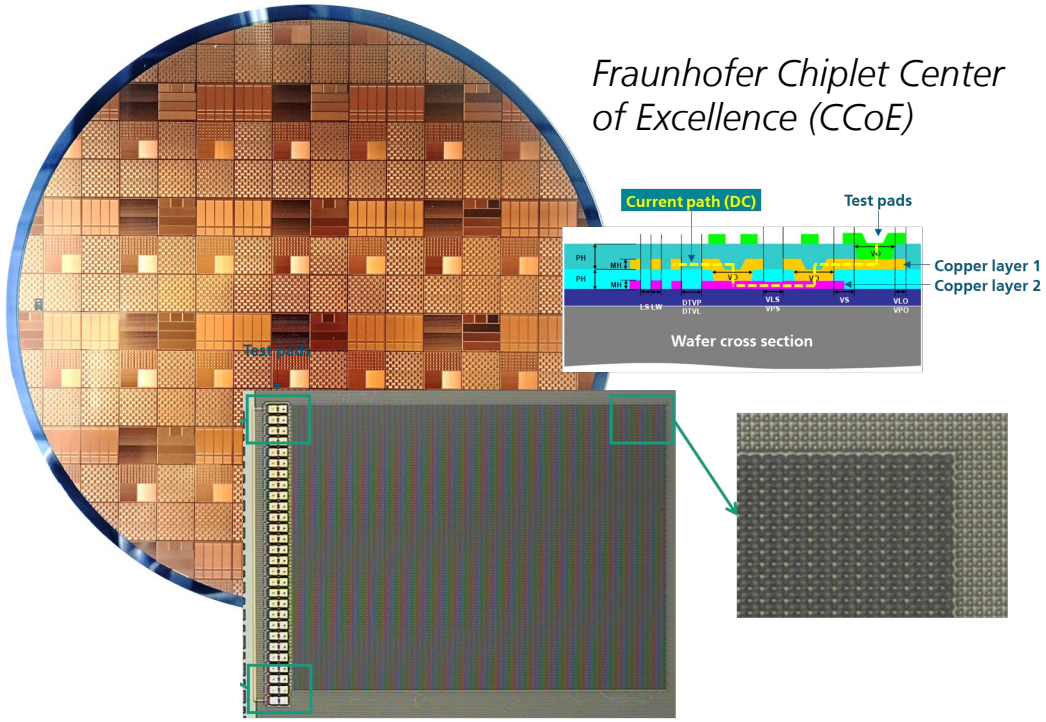


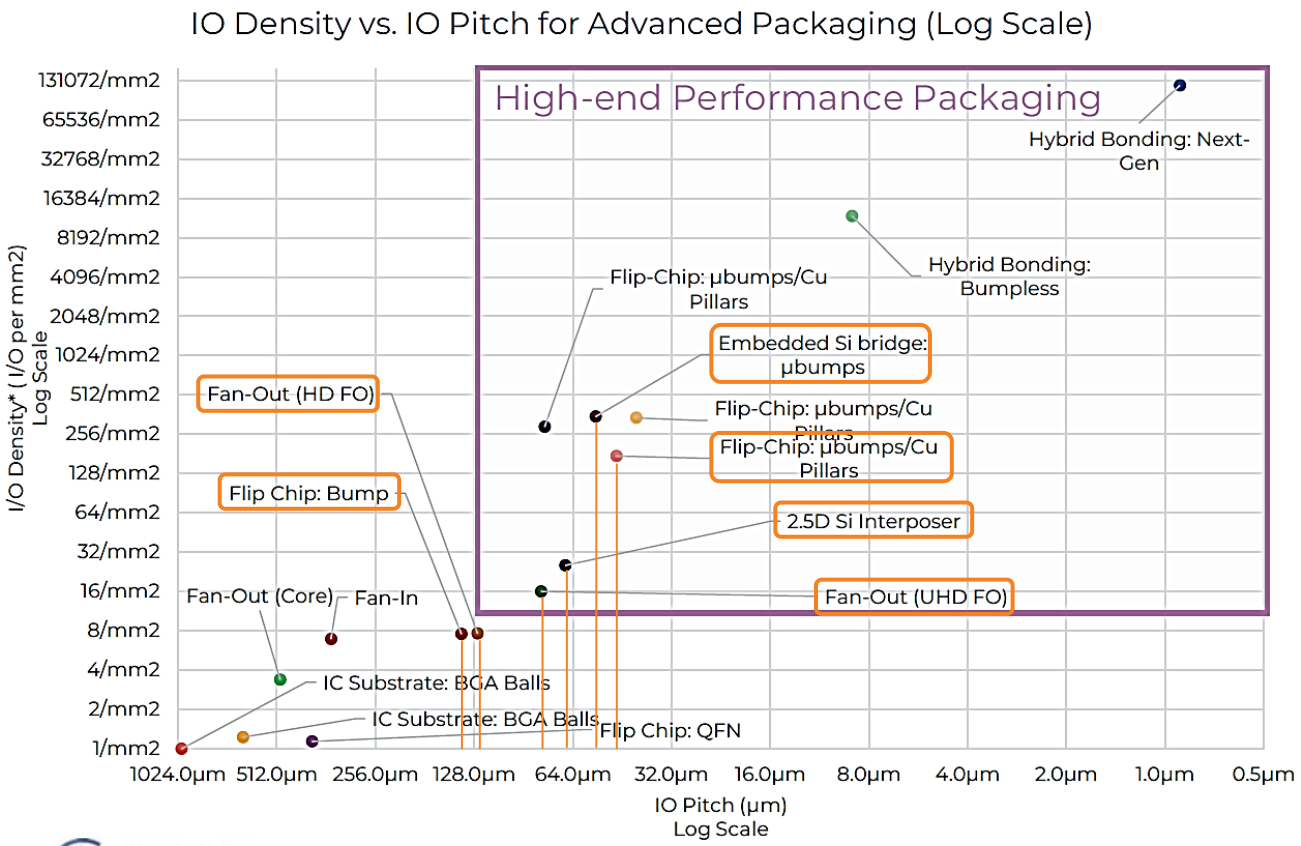




Fraunhofer Chiplet Center of Excellence (CCoE)

Fraunhofer IZM

Trends: From Substrate to Bridge Embedding to Interposer



YOLE Group

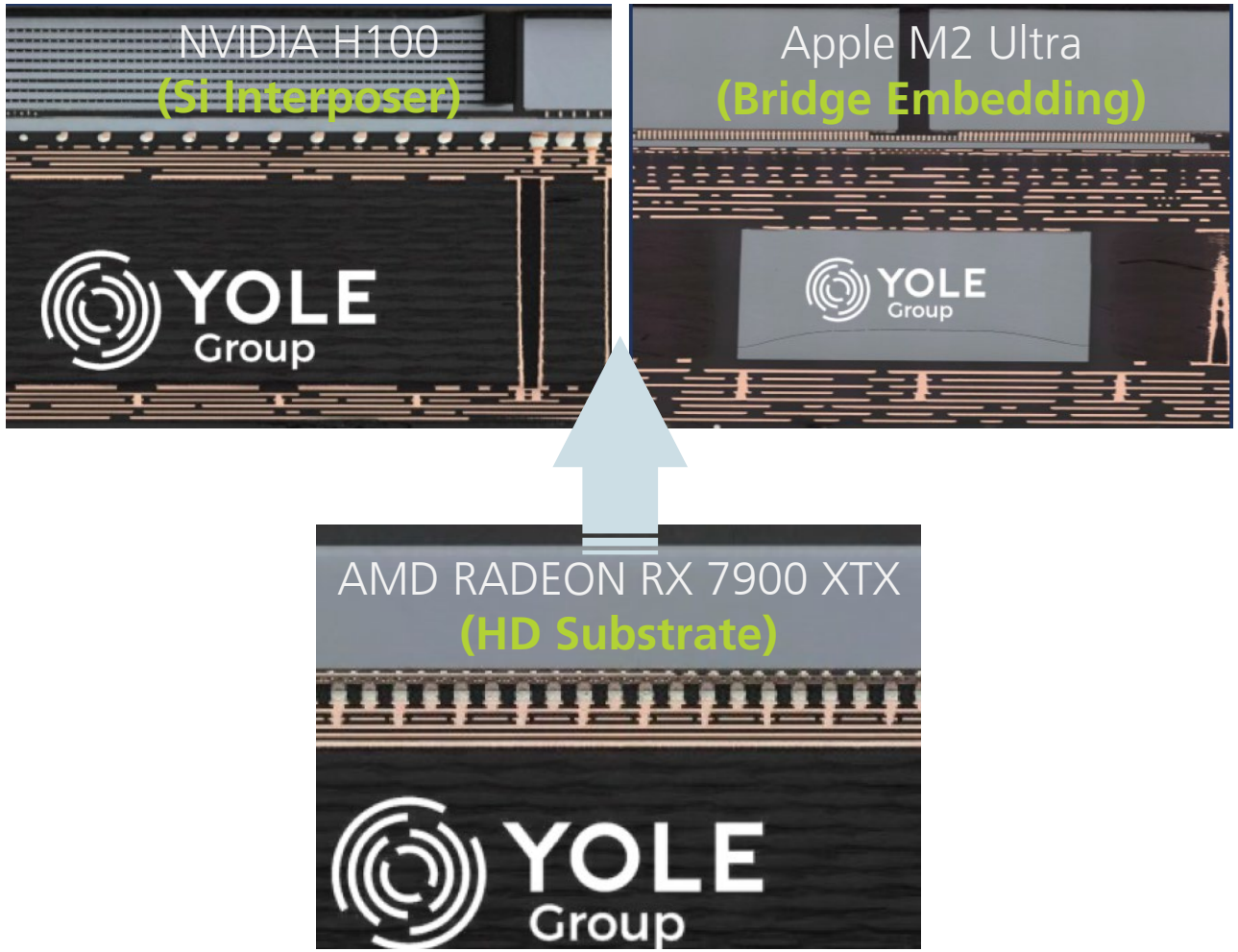
*I/O Density refers to the total number of IOs per package platform area

- ***Value Shift*** from Front-End to Back-End (60/40 ratio) esp. in the "After Moore's Law" era

- ***HD Substrate*** Bump Pitch ~100-150µm
- ***Bridge Embedding*** Bump Pitch ~40-60µm
- ***Si-Interposer*** Bump Pitch ~25-55µm

- ***Challenges***
  - Warpage due to different material CTE
  - Very thin die/bridge handling (< 60µm)
  - Dies with approx. 20x20mm² footprint
  - Assembly: TC vs. Reflow
  - Thermal management (heat spreading, cooling concepts)
  - Underfill: CUF vs. MUF vs. PUF
  - Test strategy and continuous data tracking (in-line vs. final)

Trends: From Substrate to Interposer and Bridge Embedding Packages



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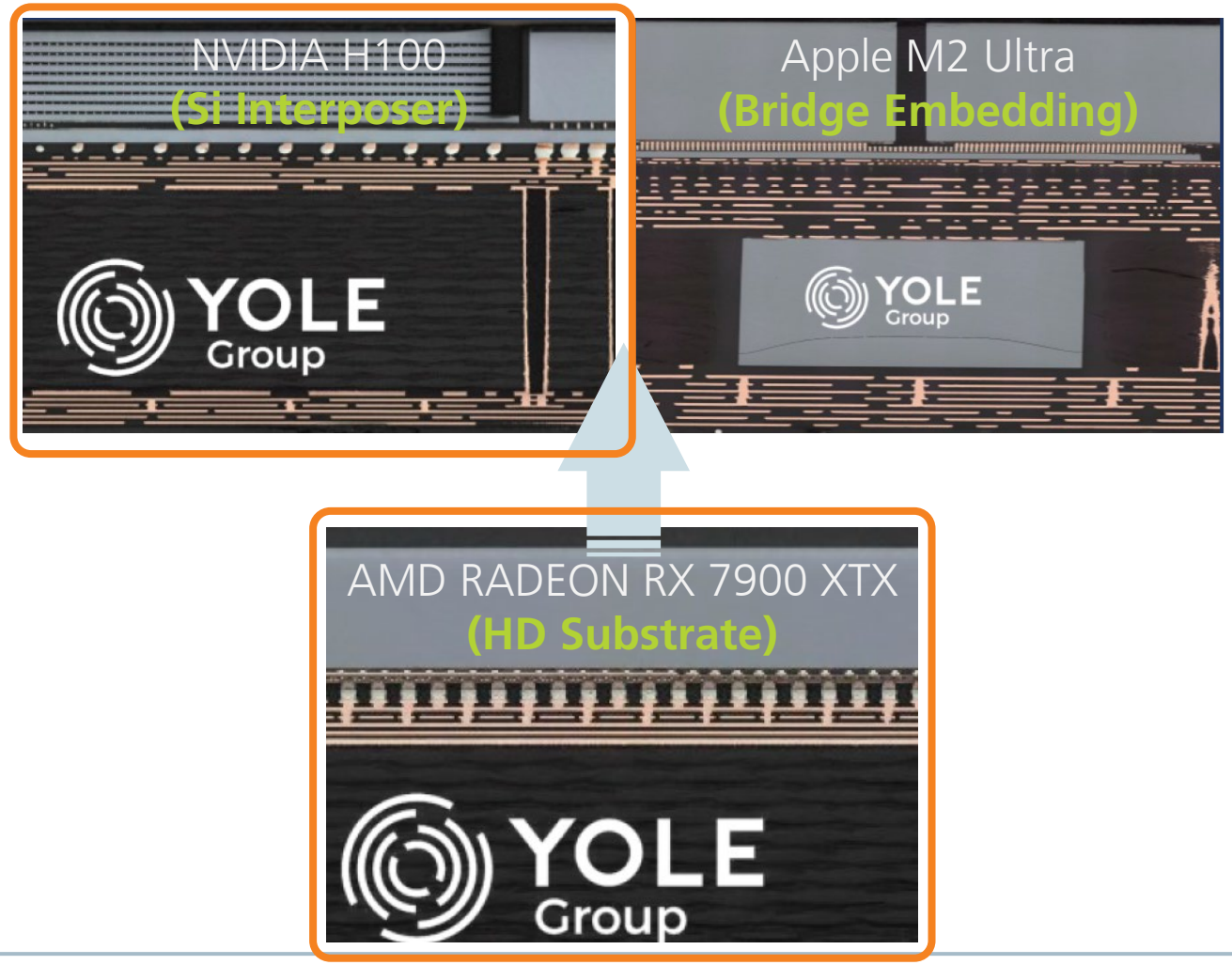

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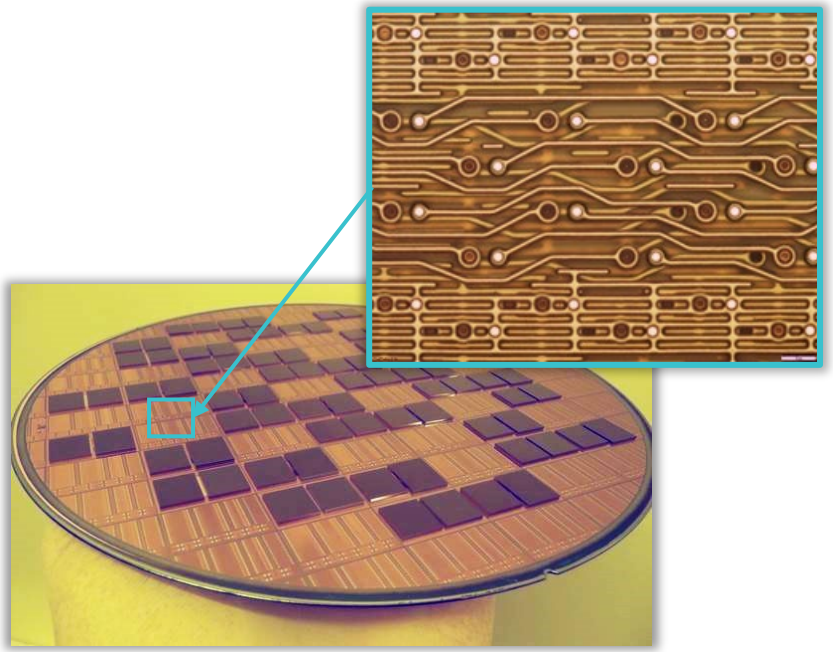
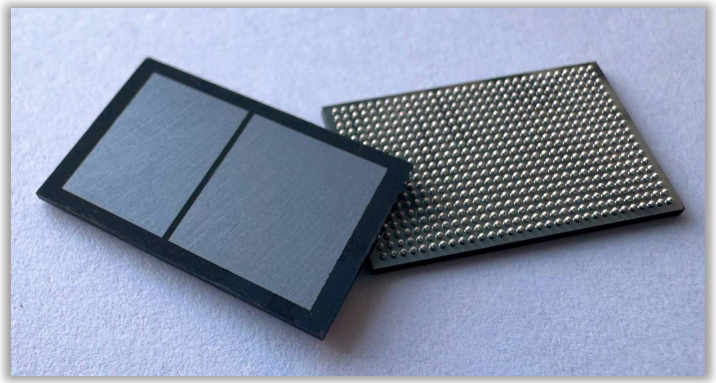
STXmod – HPC Chiplet Module Development

Fraunhofer-Funded, Duration: 2022-2025

- HPC module development incl. power and signal integrity design of inter chip communication
- Stencil/Tensor processing unit (STX) with PCIe gen5 interface, 100mm² footprint
- 16GB HBM2e (optional upgrade to HBM3)
- Silicon interposer:
  - Cu/Polymer-RDL (4M4P RDL, 4µm L/S, 6µm via), 250mm² footprint
  - I/O ball count (20x42 BGA, ball dia 300µm, ball pitch 660µm)
  - D2HBM connections: 1024 high speed data lines

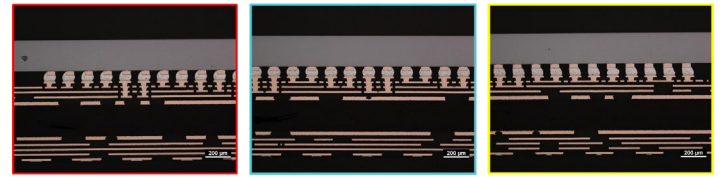


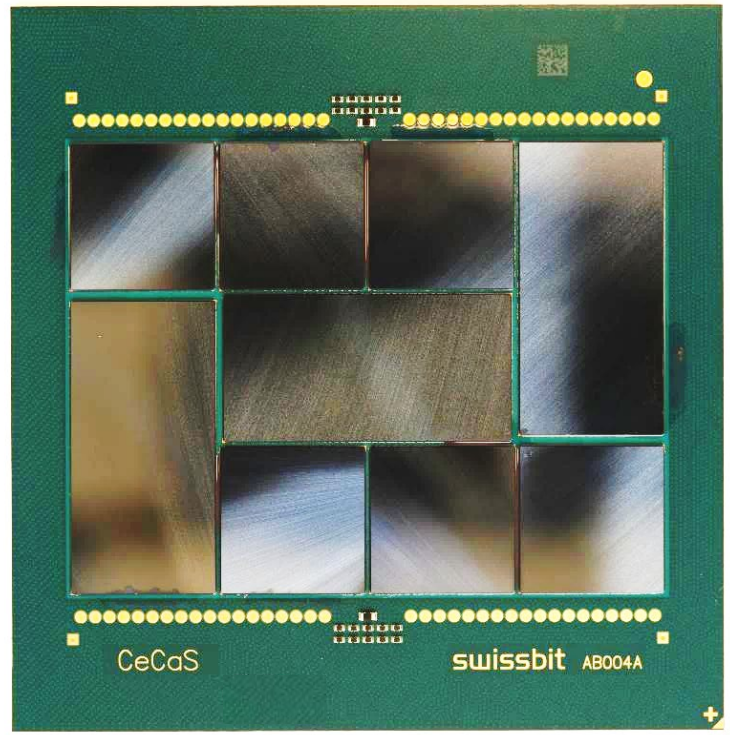


CeCaS Mannheim – Central Car Server

BMBF-Funded, Duration: 2022-2025

- Approaches for completely new automotive qualified high-performance processors for demanding control tasks in vehicles and future central car servers (TRL 2-5)
- Validation by demonstration of different chiplet modules on organic substrate
- Implementation of the entire process chain from substrate production to the assembly of chiplet modules on system PCBs:
  - Die sizes between 10x10mm² to 40x40mm²
  - balling pitches 150-300µm

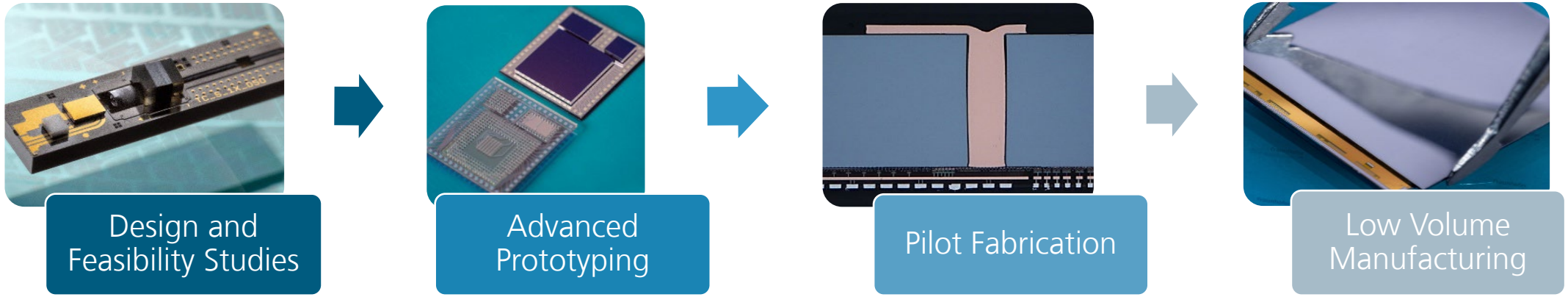




Key Messages

- The era of chiplet systems just began and gives numerous options for system realization
- Signal and power integrity is key to D2D communication
- Overall performance is increased by comprehensive system architectural approach – STCO
- The devil is in the details and needs holistic exorcism:
  feature size shrinkage - material combinations - manufacturability - performance …

…and last but not least: ***Fraunhofer IZM*** offers support along the whole value chain…



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