Fraunhofer IZM

Fraunhofer Institute for Reliability and Microintegration IZM

Electronic Packaging Days 2025

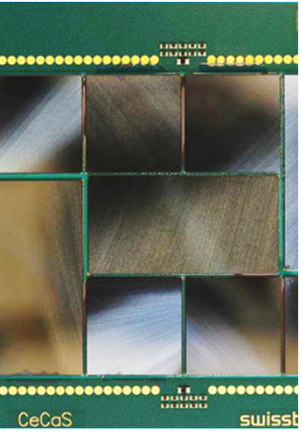
Dr. Ole Hölck

Size Does Matter

How HPC Module Form Factors Increase with Chiplet Technology

Size Does Matter:

How HPC Module Form Factors Increase with Chiplet Technology



Chiplet packaging is the key technology enabling modularity and scalability for HPC

Increasing module formats are the result of increasing demands on performance.

Large areas, high performance & 3D integration on component level lead to thermal and mechanical challenges

Cost efficiency in HVM can only be reached if panel level packaging technologies are applied

Size does matter

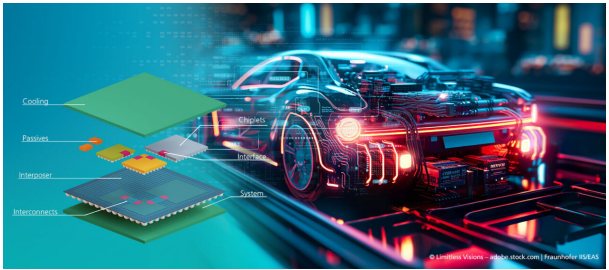
Increasing demand on performance

Automotive HP egde computing

- Real time analysis and decision making based on multiple sensor data and imaging
- High speed communication between vehicles
- High efficiency per Watt

Data Center HPC

- Scalability and flexibility in a dynamic market
- Efficient thermal- / power-management
- Robust communication infrastructure

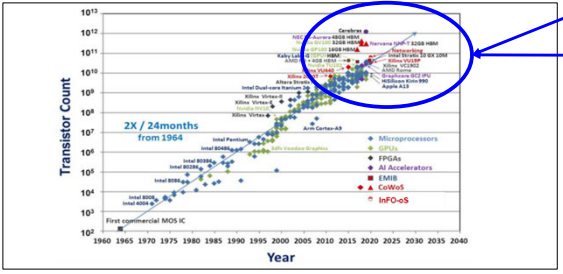


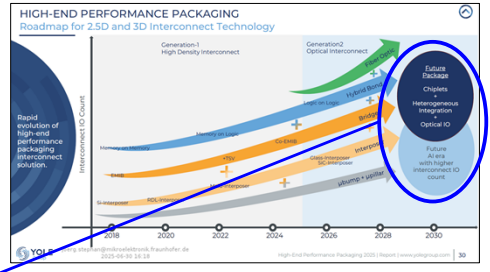
Size does matter

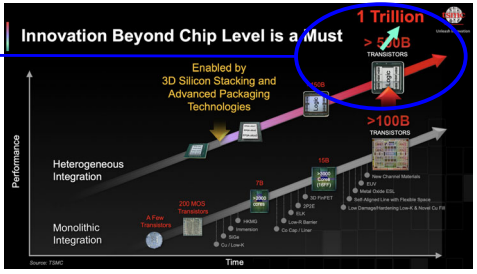
Timeline

- Moore's law slows down, reaching physical limits
- 3D integration technologies take over to boost Transistor Count / I/O Count / Performance

→ System scaling







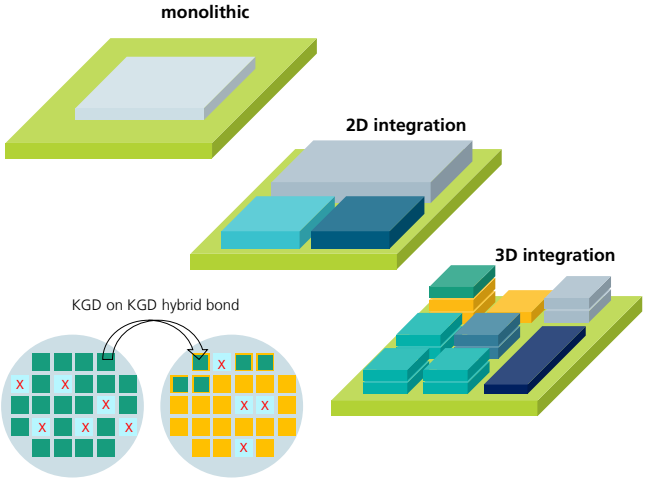
Size Does Matter

From Monolithic to 3D integration

Monolithic SoCs
- high performance
- fast communication, low interconnect power
- yield issue: system failure for 1 error per die area
- Size limitation

2D integration
- improved yield
- added flexibility
- Size limitation per chiplet, not per module
- decreased time to market
- increased interconnect length

3D integration: Quasi Monolithic Chip integration
- improved yield
- added flexibility
- decreased time to market
- decreased interconnect length (hybrid bonding)
- increased interconnection density
- More active area per substrate area
- Thermal issues



e.g. Intel EMIB and QMC technology
Johanna M. Swan, Intel

Size does matter

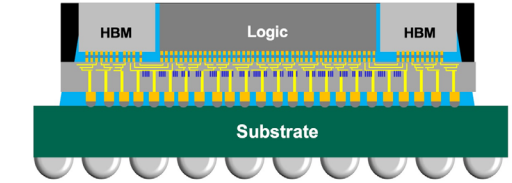
Todays High Performance Packages

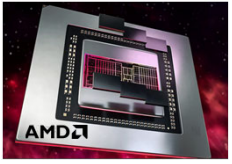
Technologies

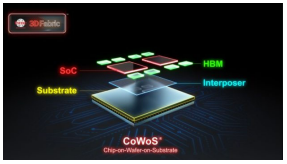
- TSMC CoWoS
- AMD RDNA 3
- Samsung I-Cube
- Tesla Dojo
- …

Applications

- AI training accellerators
- Data centers
- Gaming graphics
- 5G
- Autonomous driving
- Metaverse tech
- Medical
- …







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Size does matter

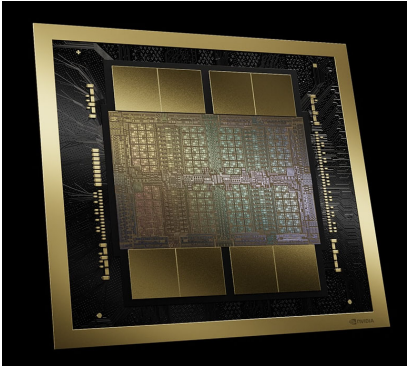
NVIDIA Referenz Data Center GPU Architecture

NVIDIA GB300 NVL72 Rack Scale System

- **Combines 36 Grace CPUs and 72 Blackwell Ultra GPUs in one rack-scale solution acting as a single GPU**
- **Highly optimized, energy efficient**
- **Cooling solution**
- **Ready to use**
- **Modular → scalability, flexibility**

BUT: Proprietary

NVIDEA Blackwell Ultra GPU

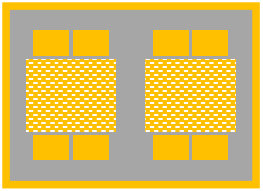


Size does matter

Towards Open Chiplet Ecosystems

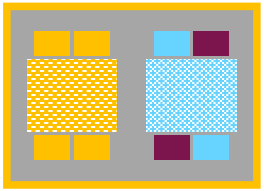
Heterogenous
Closed Chiplet Ecosystem

- **Modular: Flexible, scalable**
- **Proprietary, limited participation of market innovations**



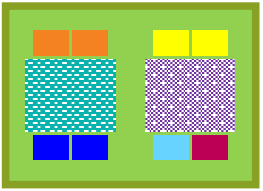
Heterogenous
Hybrid chiplet approach

- **Open interface**
- **Extendable functionality**
- **Limited customisation**
- **Limited scalability**



Heterogenous
Open Chiplet Ecosystem

- **High flexibility, scalability**
- **Customisation**
- **Market participation**
- **Innovation**

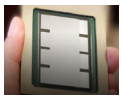


Size does matter

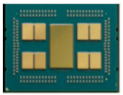
Advanced Packaging Technologies

Heterogeneous Architecture Platform (Technology Building Blocks)

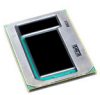
- 2D / 2,5D
  - Interposer
    - Silicon
    - Organic
    - Glass
  - Fan-out
  - Embedded Si/glass Bridge
- 3D
  - µBumps or Hybrid Bonding
    - SoC Stacking
    - Memory Stacking



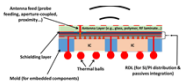
Si Interposer
Source: TSMC



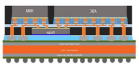
Organic Interposer
Source: AMD



Glass Core Interposer
Source: INTEL

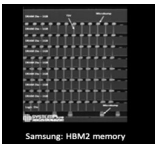


Fan-out, Source: FhG-IZM



Si-Bridge, Source: ASE

Hybrid Bonding,
Source: INTEL



Source: SystemPlus

Chiplet Architecture Revolution

Different technology building blocks can be used for Chiplets

Chiplets will be a key enabler for next 10-15 years

Source: AMD, Overclock3D.net

for HPC, AI, Automotive, Industrial Automation, 5G/6G, Health Care, Energy, Aerospace, ...

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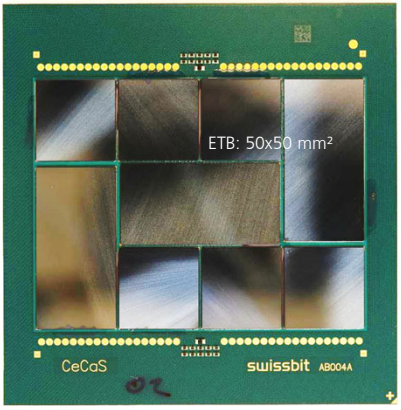
Fraunhofer IZM participation example

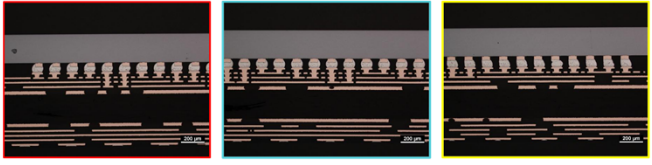


CeCaS – Central Car Server
Supercomputing platform for fully automated vehicles

- **Development of software and hardware for future automotive control units**
- **Realisation of heterogenous chiplet modules to optimize assembly processes and derive**

- **Assembly Design Kits (ADK)**
- **Thermal Management Strategies**
- **Reliability Models**

→ Towards a Compact Digital Twin



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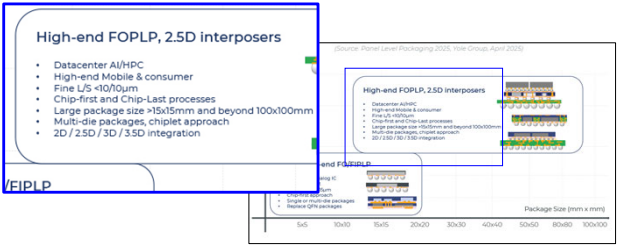
Yole reports 2025



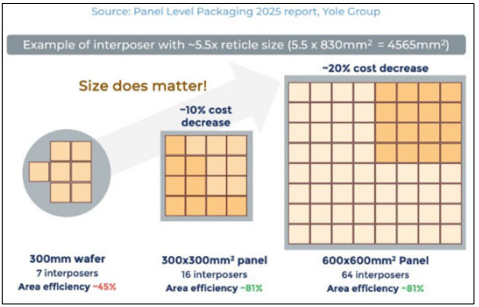
Yole reports on

Panel Level Packaging

High-End Performance Packaging

Main Drivers to adopt Panel Level Packaging

- …
- Large package sizes (>15 x 15 mm² and beyond 100x100 mm²)
- Multi-die packages (chiplet approach)
- …
- Area efficiency
- **Cost reduction**



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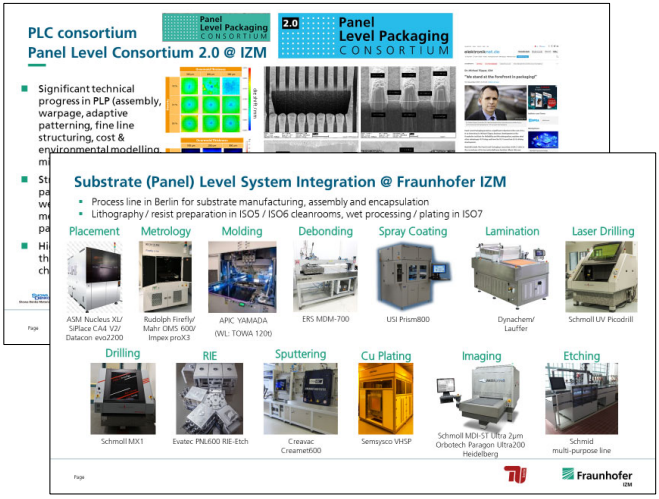
Panel Level Packaging @ Fraunhofer IZM

- **Leadership of industrial consortium PLP and PLC2.0 until 202**
- **Process line for substrate manufacturing, assembly and encapsulation**
- **New equipment in procurement → APECS pilot line**



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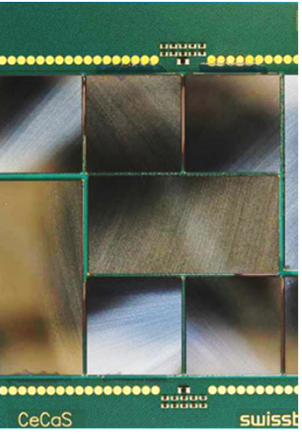

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Thank you for your attention

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