Fraunhofer
IZM

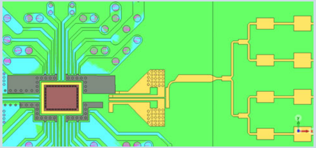
Fraunhofer Institute for Reliability
and Microintegration IZM

**Electronic Packaging Days 2025**

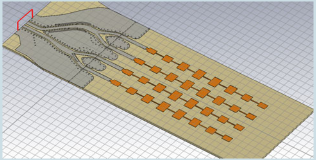
**Dr. Alexander Gäbler**

# **High-Speed Design**, Fabrication and Assembly of Interposers on System Boards for Chiplets and HPC

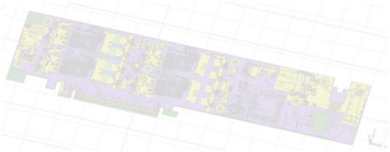
# RF and High Speed Design



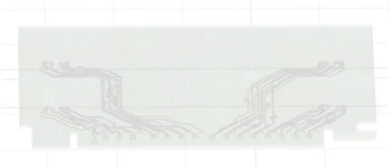
- Radar Module



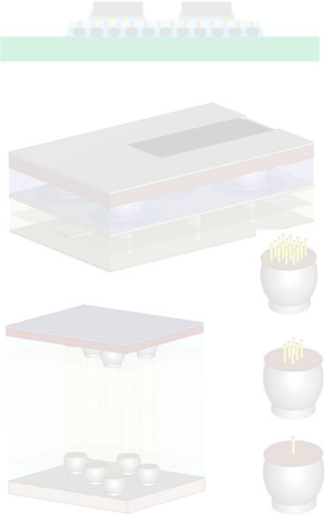
- **5/6G Frontend Modules**



- High Performance Computing Bord



- PCB / High Speed Design

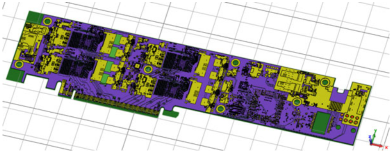


- Packaging concepts / Layout

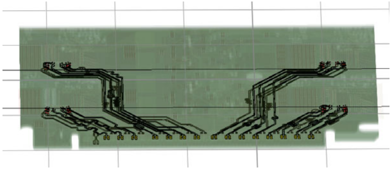
# RF and High Speed Design

**High Speed Signal Transmission**

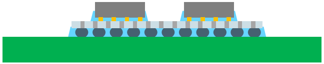
- Chip to Chip
  - UCI
  - HBM
- Chip to Bord
  - PCI 5th Gen (32GBit/s)
- Signal Integrity
- Power Integrity

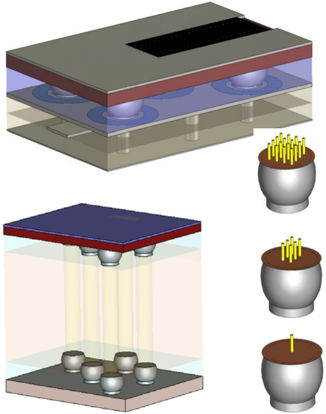


- High Performance Computing Board (HPC)



- PCB / High Speed Design





- Packaging concepts / Layout

# Design Flow

## Requirements

Elaboration of System Requirements

RF-Design und time domain analysis of signal paths

Architecture und Optimization

JEDEC STANDARD

High Bandwidth Me
(HBM1, HBM2)

JESD235D
(Revision of JESD235C, January 20

FEBRUARY 2021

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

JEDEC

Micron Confidential and Proprietary

Micron

16GB HBM2E DRAM
Features

HBM2E DRAM

MT54A16G808A00AC — 8 channels × 128 Meg × 144 I/O

Features

Options[1]

Marking

Verification by Time Domain Analysis, Redesign (if needed)

Metrological Characterization of Components and Test Structures

Layout and Manufacturing of Functional and testable Structures

Fraunhofer IZM

# Design Flow

## Signal Integrity

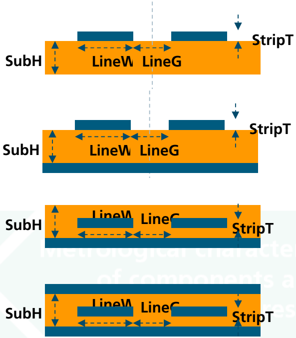
Elaboration of System Requirements

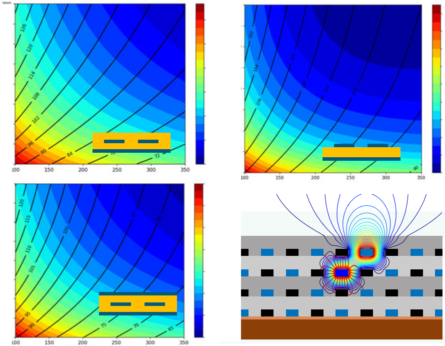
RF-Design und time domain analysis of signal paths

Architecture und Optimization

### Software / Toolchain

- Altium
- HFSS
- CST
- Cadence
- Self Dev. Tools (based on Matlab, Python, etc.)





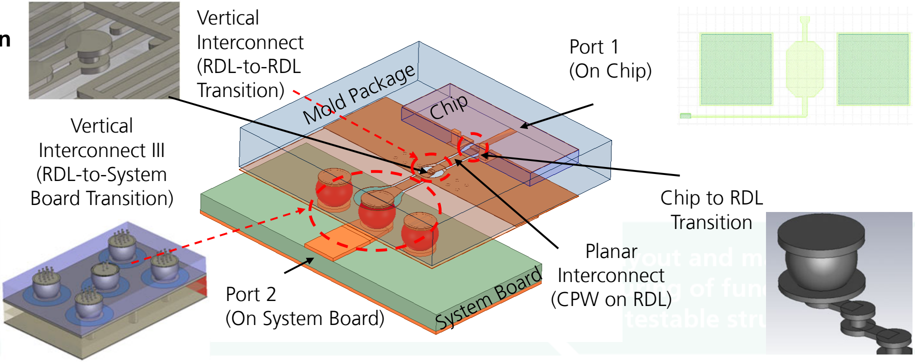
# Design Flow

## Signal Integrity

Elaboration of System Requirements → RF-Design und time domain analysis of signal paths → Architecture und Optimization

**Software / Toolchain**

- **Altium**
- **HFSS**
- **CST**
- **Cadence**
- **Self Dev. Tools (based on Matlab, Python, etc.)**



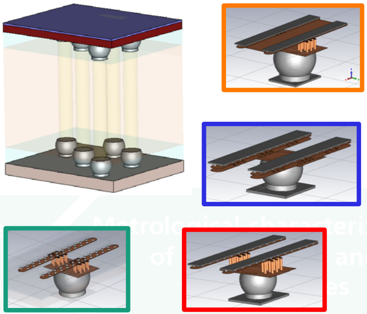
# Design Flow

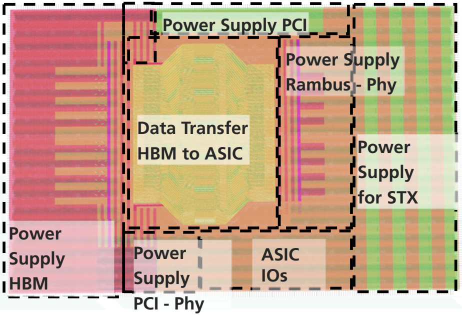
## Power Integrity

Elaboration of System Requirements → RF-Design und time domain analysis of power supply → **Architecture und Optimization**

**Software / Toolchain**

- **Altium**
- **HFSS**
- **CST**
- **Cadence**
- **Self Dev. Tools (based on Matlab, Python, etc.)**





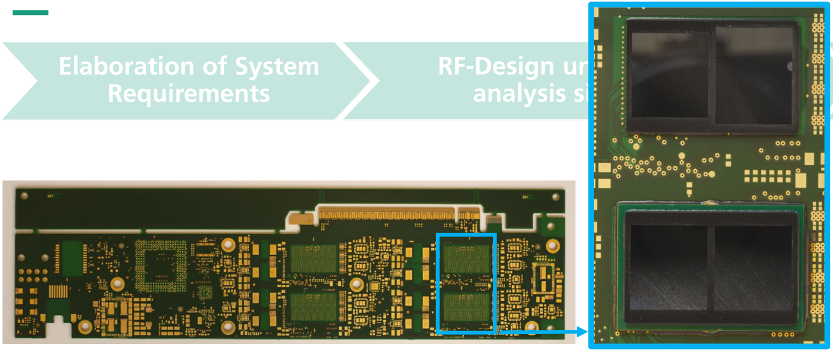
# Assembly

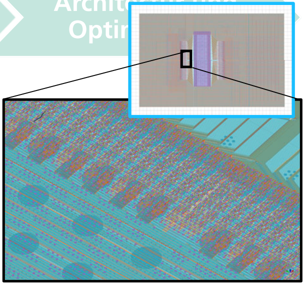
## Chiplet to PCB

Elaboration of System Requirements

RF-Design un
analysis si

Archite
Optir





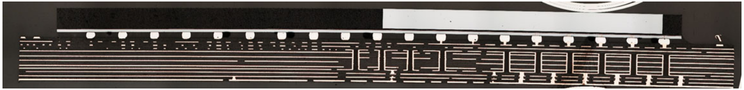
Layout and Manufacturing of Functional and testable Structures

Metrological Characterization of Components and Test Structures

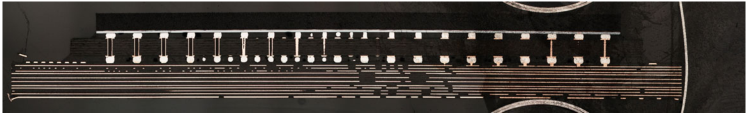
Verification by Time Domain Analysis, Redesign (if needed)

# Assembly

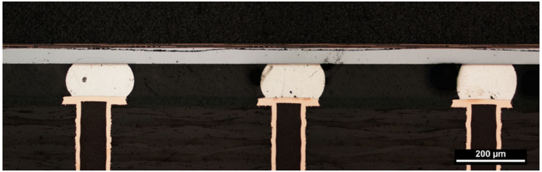
## Chiplet to PCB

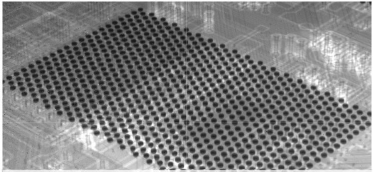


**Package on PCB**

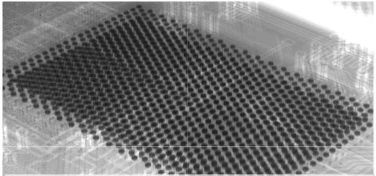


**Package on Low CTE and PCB**





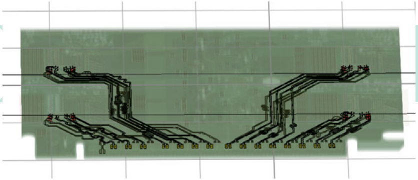
**X-Ray images of Package on PCIe**
**No Abnormalities visible**

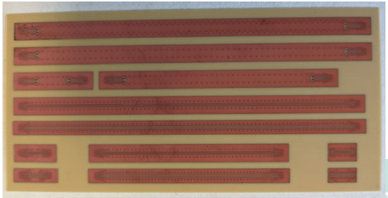


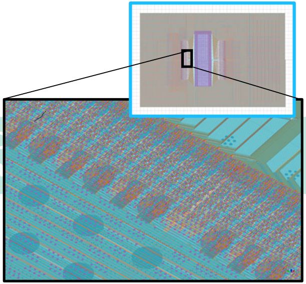
**X-Ray image of Package on Low CTE Interposer on PCIe Board**

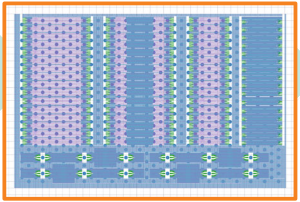
# RF Test Structures

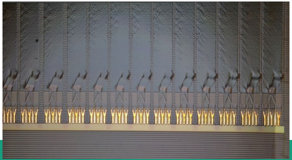
RF-D
a











**PCB Components**

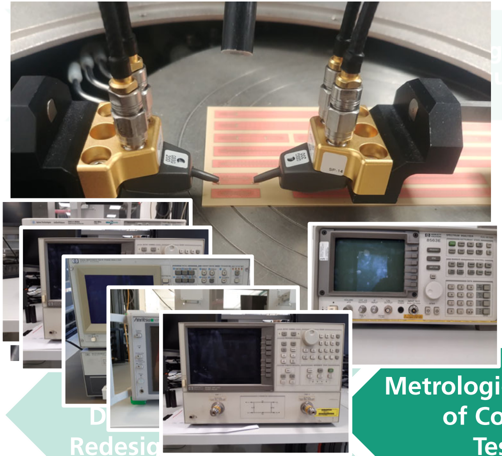
**Chiplet Components**

Layout and Manufacturing of Functional and testable Structures

Metrological Characterization of Components and Test Structures

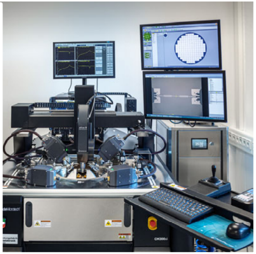
Verification by Time Domain Analysis, Redesign (if needed)

# Measurement Capabilities at IZM



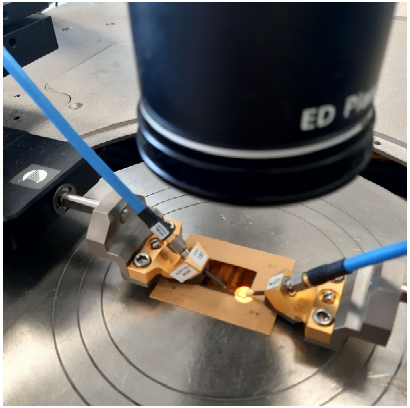
- Arbitrary Function Generator
- Bit Error Rate Tester
- EMC / Antenna Measurements up to 320 GHz
- S-Parameter Measurement up to 510 GHz

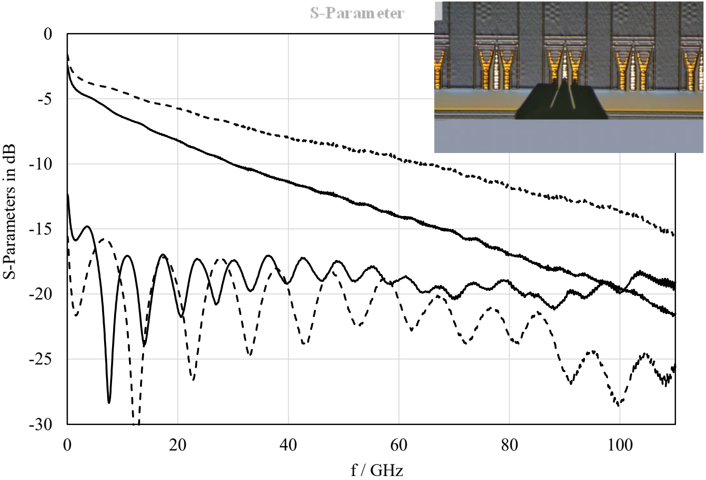
Metrological Characterizatio
of Components and
Test Structures



# Measurement and Evaluation

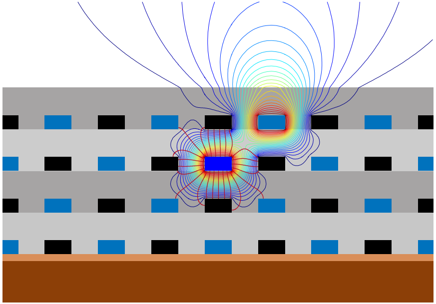
## Signal Path Measurement of single ended or differential lines up to 110 GHz

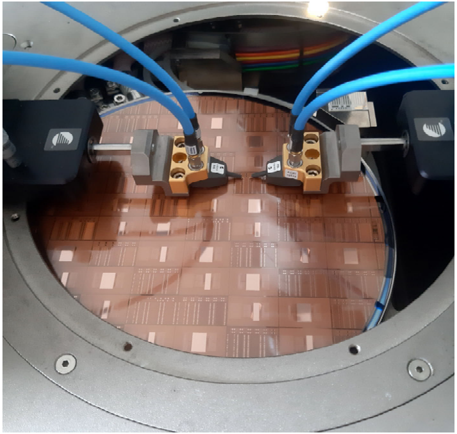




# Measurement and Evaluation

## Cross talk evaluation





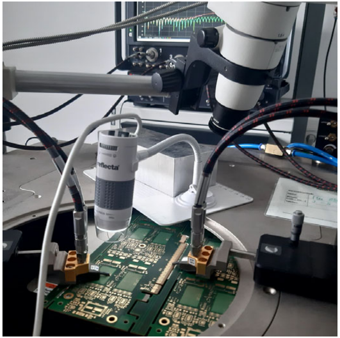
Verification by Time Domain Analysis, Redesign (if needed)

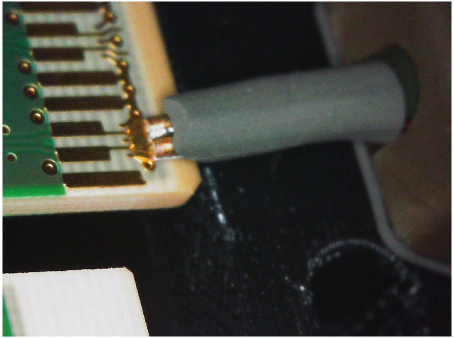
**Metrological Characterization of Components and Test Structures**

Layout and Manufacturing of Functional and testable Structures

# Measurement and Evaluation

## Signal Path Measurement of differential PCI Lanes





**Verification by Time Domain Analysis, Redesign (if needed)**

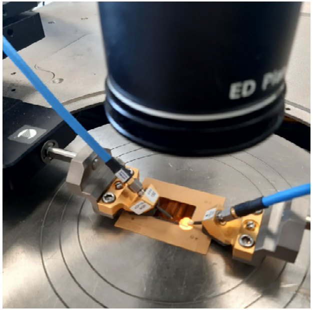
**Metrological Characterization of Components and Test Structures**

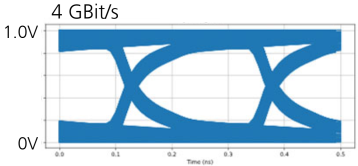
**Layout and Manu-facturing of Functional and testable Structures**

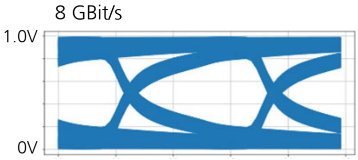
Fraunhofer IZM

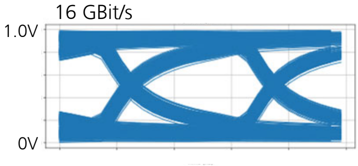
# Measurement and Evaluation

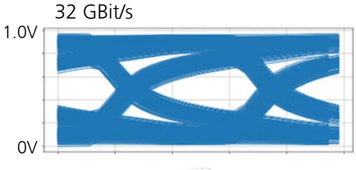
## Eye Diagrams

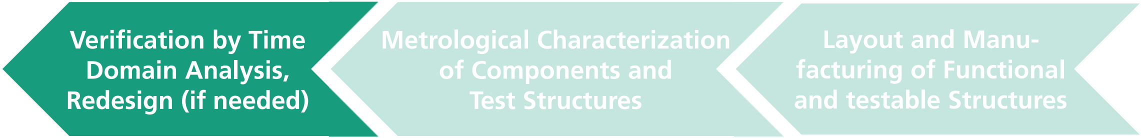



4 GBit/s


8 GBit/s


16 GBit/s


32 GBit/s


Verification by Time Domain Analysis, Redesign (if needed)

Metrological Characterization of Components and Test Structures

Layout and Manufacturing of Functional and testable Structures