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Fraunhofer Institute for Reliability and Microintegration IZM

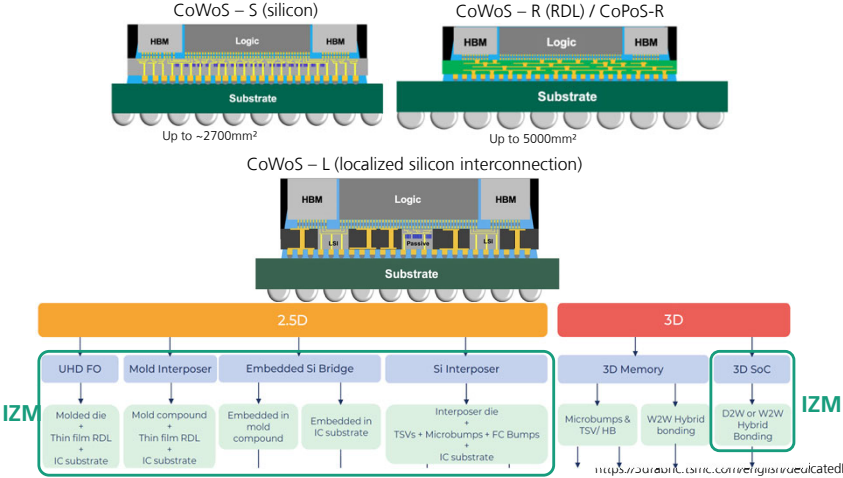
Electronic Packaging Days 2025

Markus Wöhrmann

High-End Performance Packaging - Latest Trends

HPC – Packaging

HPC Packaging family at TSMC (Chip on Wafer/Panel on Substrate)



https://3dfabric.tsmc.com/english/dedicatedFoundry/technology/cowos.htm

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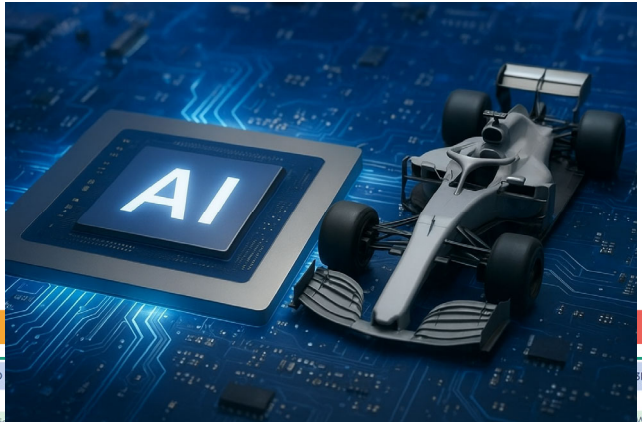
HPC – The Formula one of packaging technology

HPC Packaging family at TSMC (Chip on Wafer/Panel on Substrate)



Does everyone need HPC Packaging?

No, but everyone likes ABS

https://3dfabric.tsmc.com/english/dedicatedFoundry/technology/cowos.htm

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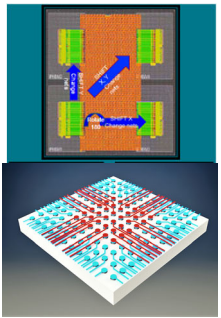
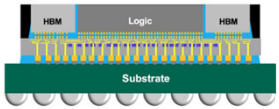
HPC - Chip on Wafer on Substrate Packages

D2D routing demand



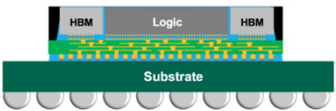
HPC Packaging family at TSMC (Chip on Wafer/Panel on Substrate)

CoWoS – S (silicon)



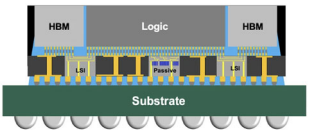
Up to ~2700mm²

CoWoS – R (RDL) / CoPoS-R

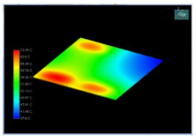


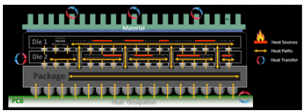
Up to 5000mm²

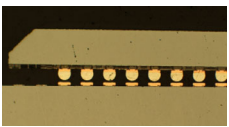
CoWoS – L (localized silicon interconnection)



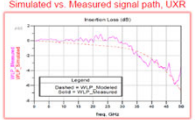
Thermal management







Signal/ Power integrity



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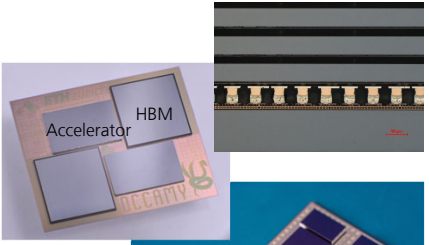
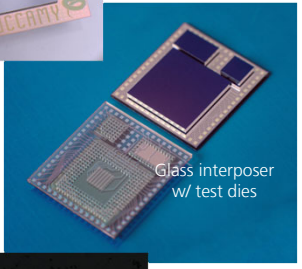
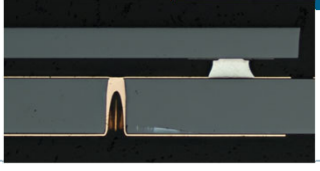
D2D - Interposers as platform for Chiplets

Silicon, Glass and Silicon Carbide

- **Si-interposers** w/ polymer based RDL and TSV → established technology, approved by industry
- **Glass interposers** → technology path explored, various TGV and cavity options, interest from industry (FAMES Pilot-line)
- **SiC interposers** → w/ polymer based RDL and TSV → heat dissipation and stiff interposer







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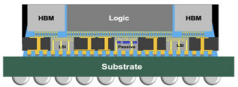
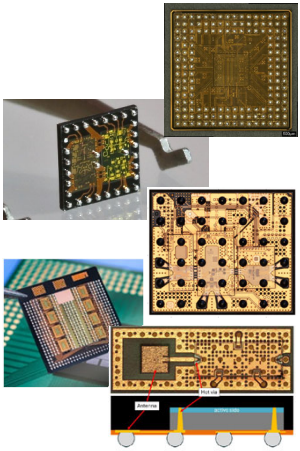
D2D - Fan Out Wafer Level Package (FOWLP)

CoWoS – L (localized silicon interconnection)





Chip First

Face-DOWN „eWLB“

Apply thermal release tape on carrier

Face-down die assembly on carrier

Wafer/panel overmolding

Carrier release

RDL (e.g. thin film, PCB based, …), balling, singulation

Chip Last

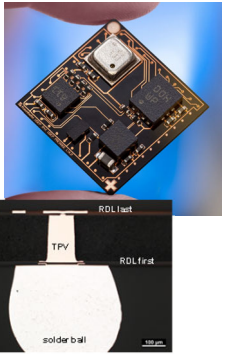
Apply release layer on carrier

RDL (e.g. thin film, PCB based, …)

Die assembly on carrier

Wafer/panel overmolding

Carrier release, balling, singulation



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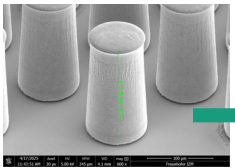
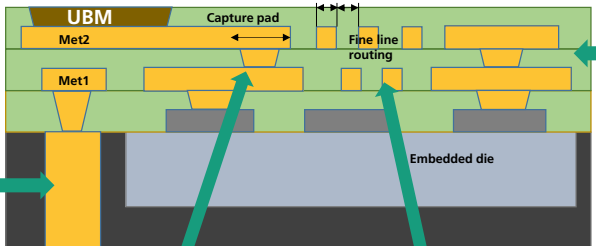
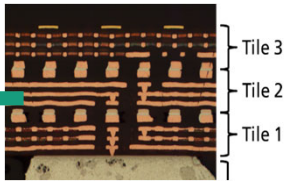
D2D - routing demand and 3D packaging

Tall pillar plating



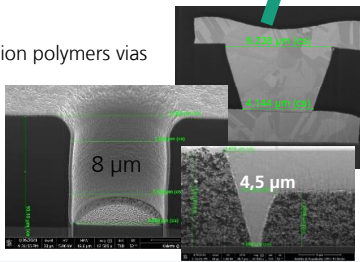


Multi-layer processing

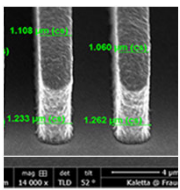


IZM multi-RDL stacking (35mmx35mm) with 9 layers of 8 um L/S – organic interposer

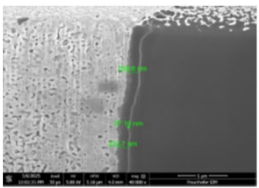
High resolution polymers vias



Fine line routing



Barrier integration



Cu-ion migration stability

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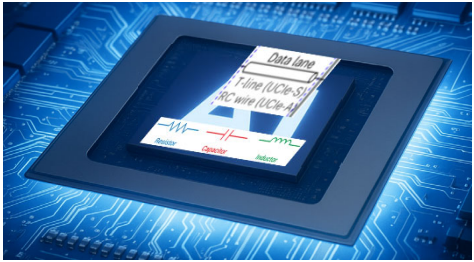
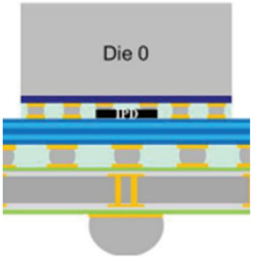
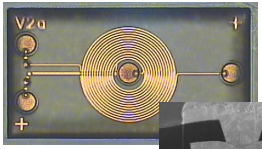
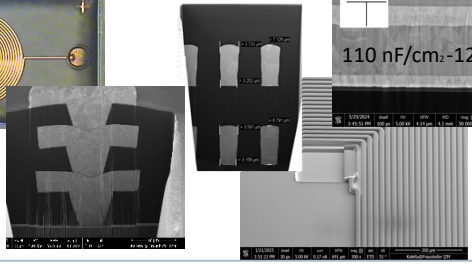
Signal/Power Integrity

- High frequency **Chiplet communication**
- **Power stabilty/ voltage management** close to the dies
- **Passive integration** in polymer interposers
- **RF Characterization** of RDL materials
- **RF optimized** stacking from layer to layer vias



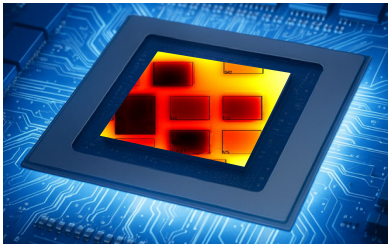




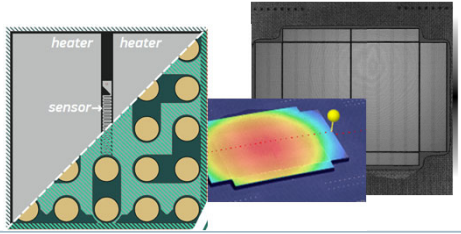


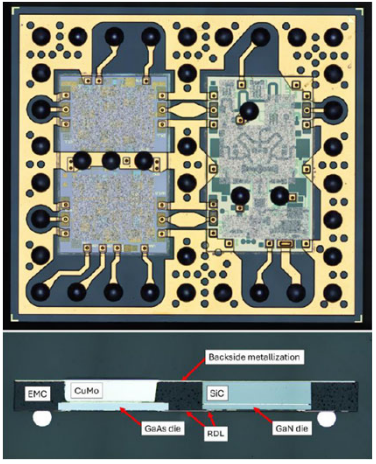
Thermal Management

- Application of innovative technologies for **improved cooling concept**
- **Warpage** evaluation and **stress** management
- **Material characterization/ evaluation**
- **Thermal management evaluation**



Thermal test chip >11W/mm²





Fan Out of HPA and LNA in one package

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NANOTEST Berliner Nanotest und Design GmbH

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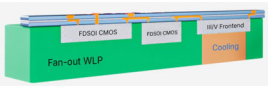
Summary and Outlook

APECS – IZM as part of the pilot line

- Establish HPC packaging capabilities in europe, which is based on interposers, bridges and FanOut technology
- Establish the access to advanced packaging for european SMEs
- Support material and process developments
- Innovations in characterization of materials / packages



APECS Demonstrator: Multi MMIC chiplet embedding using Fan-out Wafer Level Packaging (FOWLP) with backside cooling

Chips JU
Co-funded by the European Union
With funding from the: Federal Ministry of Research, Technology and Space
SACHSEN BERLIN Bayerische Staatsregierung SH
Baden-Württemberg LAND BRANDENBURG SACHSEN-ANHALT

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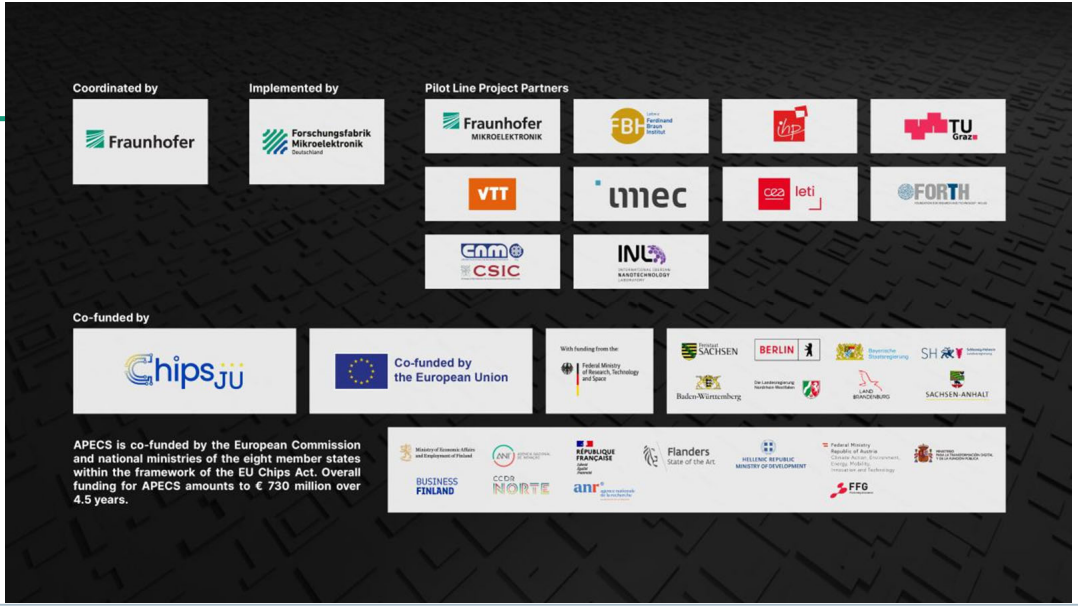
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Co-funded by the European Union
With funding from the:
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APECS is co-funded by the European Commission and national ministries of the eight member states within the framework of the EU Chips Act. Overall funding for APECS amounts to € 730 million over 4.5 years.
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Kontakt

Markus Woehrmann
Lithography and Thin Film Polymer
Wafer Level System Integration (WLSI)
Phone: +49 30 46403-617
E-Mail:
Markus.woehrmann@izm.fraunhofer.de

Fraunhofer IZM Berlin
Gustav-Meyer-Allee 25
13355 Berlin
Germany
+49 30 46403-100

Fraunhofer IZM-ASSID
Ringstraße 12
01468 Dresden-Moritzburg
Germany
+49 351 795572-12

Fraunhofer IZM Außenstelle Cottbus
Karl-Marx-Straße 69
03044 Cottbus
Germany
+49 355 383 770-12

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