

Electronic Packaging Days 2025

# Energy and Carbon Footprint of Advanced Computer Hardware for HPC and AI Systems

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Dr. Lutz Stobbe,  
Fraunhofer IZM, 2025 Electronic Packaging Days, November 6th 2025

# Gigawatt data center area is in full swing

Massive demand in energy and hardware

## xAI Colossus (Elon Musk)

- 1 Gigawatt power demand
- 550,000 to 1,000,000 high-end Nvidia GPUs
- Investment of 20 to 30 Billion USD on:
  - Silicon (Compute & Network) 57%
  - Power (Gas & Batteries) 20%
  - Cooling (Water Recycling) 15%
  - Real Estate (Facility) 10%



x 10

<https://www.youtube.com/watch?v=RxuSvyOwVCI>

## Stargate (OpenAI, Oracle, Softbank)

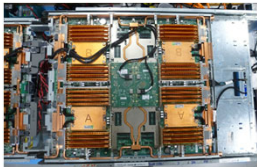
- 10 Gigawatt power demand (planned)
- Up to 10,000,000 high-end Nvidia GPUs
- Investment of 500 Billion USD announced:



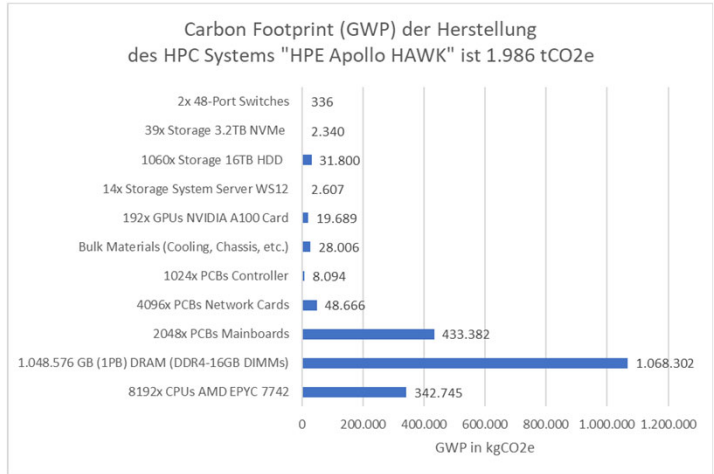
# Simplified carbon footprint assessment of the HPE Apollo HAWK System

HRLS High Performance Computing Center Stuttgart (2020 – 2025)

- 26 Petaflops (theoretical)
- 32 Racks / 4096 Compute Nodes
- ~ 3000 kW power / ~ 115 kW/PFLOP (use)
- ~ 76 tCO<sub>2</sub>e/PFLOP (manufacturing)



DRAM

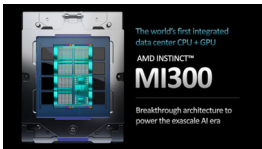


<https://www.hrls.de/de/loesungen/systeme/hpe-apollo-hawk>

# Simplified carbon footprint assessment of the HPE Cray EX4000 HUNTER

HRLS High Performance Computing Center Stuttgart (2025 -

- 48 Petaflops (theoretical)
- 8 Racks / 512 Compute Nodes
- ~ 560 kW power / ~ 12 kW/PFLOP (use)
- ~ 13 tCO<sub>2</sub>e/PFLOP (manufacturing)



DRAM



APU incl. HBM



The Carbon Footprint (GWP) of the Manufacturing of the HPC-System "HPE Cray EX4000 HUNTER" is 618 tCO<sub>2</sub>e

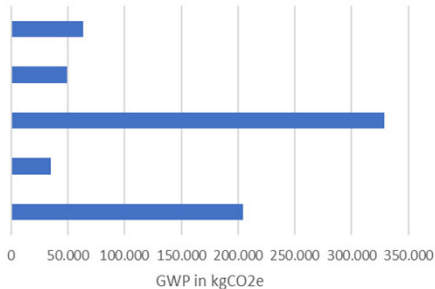
25 PB of Storage 2120 HDD (12TB)

512x Mainboard with passives & connectors

393.216 GB of DRAM DDR5-4800 ECC-Memory

512x CPU AMD EPYC Genoa 9374F

752x APU AMD Instinct MI300A



Quelle: <https://www.hlr.de/de/loesungen/systeme/hunter>

# Increasing die area of advanced processor systems

Multiple compute chip-lets with an I/O orchestrator and high bandwidth memory (HBM) in a package

Intel Xeon 8180

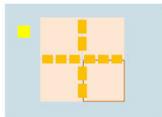
2017



Die-Area:  
6,9 cm<sup>2</sup>

Intel Xeon 8468H

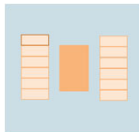
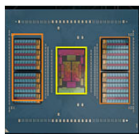
2023



Die-Area:  
21,8 cm<sup>2</sup>

AMD EPYC 9965

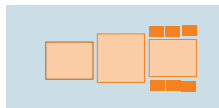
2024



Die-Area:  
14,6 cm<sup>2</sup>

NVIDIA GH200

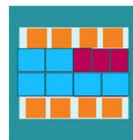
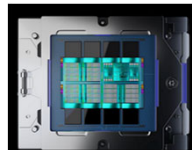
2024



Die-Area:  
45,2 cm<sup>2</sup>

AMD INSTINCT MI300

2023



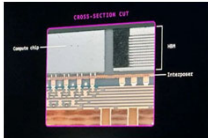
Die-Area:  
64,8 cm<sup>2</sup>

# Die-Area of application specific AI systems (ASIC) needs further analysis

## Komplexe Chiplet Systeme

### AWS Trainium 2

2024 (ASIC)



**Total die area (est): 67,8 cm<sup>2</sup>**

4x12 HBM dies: 52.8 cm<sup>2</sup>

2x ASIC dies: (15.0 cm<sup>2</sup>)

2x active Interposers: 24 cm<sup>2</sup>

### Microsoft Maia 100

2024 (ASIC)



**Total die area unknown yet**

SoC size: 8.2 cm<sup>2</sup>

64 Tiles: 4 Tiles/cluster 16 Cluster/SoC

Assumption: @ 0,8cm<sup>2</sup>/tile = **51 cm<sup>2</sup>**

### Google TPU v4

2024 (ASIC)



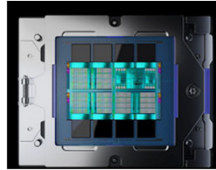
**Total die area unknown yet**

# Hardware demand for advanced computer systems

## Exemplary calculation of die area demand of an AI system

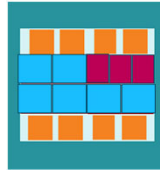
### Average XPU die area:

- 15 - 25 cm<sup>2</sup> Compute (APU, GPU, CPU)
- 40 – 60 cm<sup>2</sup> High Bandwidth Memory (HBM)
- 200 - 500 cm<sup>2</sup> Memory (DRAM)
- 25 - 40 cm<sup>2</sup> Silicon Interposer
- +++ NAND storage



**AMD INSTINCT MI300**

2023 (APU)



**Total die-area (est.): 76.5 cm<sup>2</sup>**

4x base layer dies: 14.8 cm<sup>2</sup>

8x4 HBM dies: 46.5 cm<sup>2</sup>

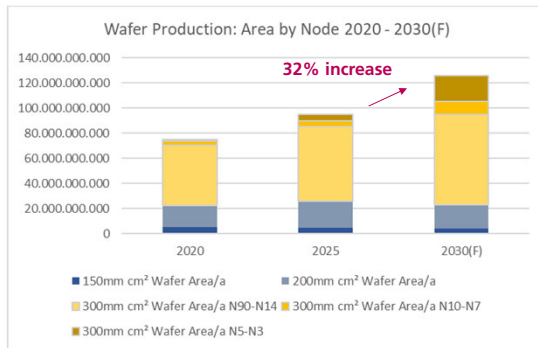
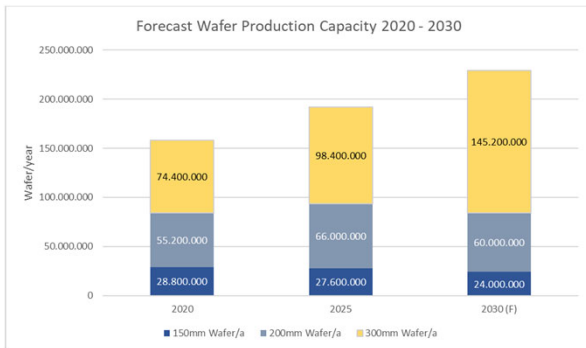
6x GPU dies: 11.5 cm<sup>2</sup>

3x CPU dies: 3.7 cm<sup>2</sup>

1x silicon Interposer: 30 cm<sup>2</sup>

# Forecast wafer production capacity 2020 to 2030

Wafer area (in cm<sup>2</sup>) is expected to increase by 32% between 2025 and 2030



Calculation by IZM based on data from:

<https://www.toolsresearch.com/12-inch-semiconductor-wafers-sell-well/>

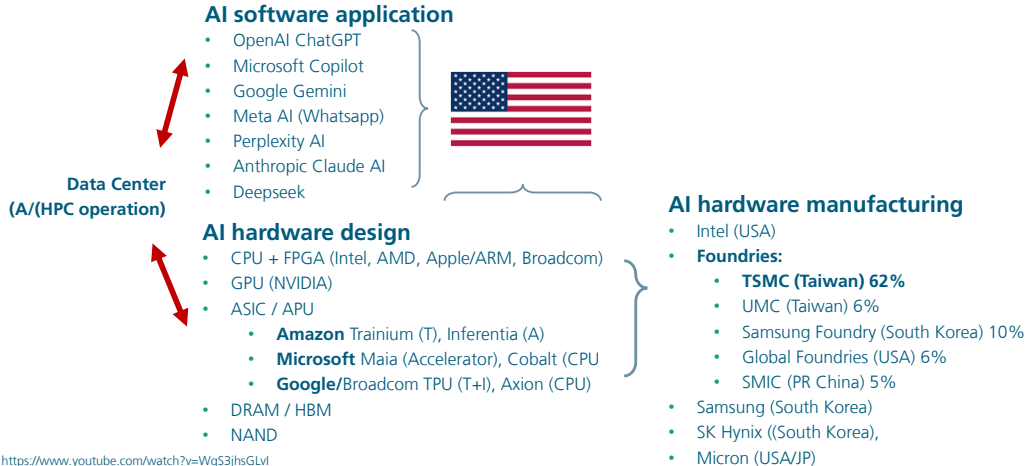
<https://www.semi.org/en/news-media-press-releases/semi-press-releases/global-semiconductor-fab-capacity-projected-to-expand-6%25-in-2024-and-7%25-in-2025-semi-reports>

<https://www.kbvresearch.com/semiconductor-wafer-market/>



# Advanced Computing (HPC/AI) is dominated by the USA

Taiwan and South Korea are currently critical links in the advanced IC supply chain



# Semiconductor manufacturing Green House Gas Protocol

Breakdown of items according to studies from McKinsey & Company and Boston Consulting Group

## Scope 2

- Electricity from the grid (consider type of energy mix)
- Heating
- Onside power plant / renewable

Average 50 - 55%

## Scope 1

- Direct emissions from process gases (consider abatement)
- Direct emissions from onside power plant

Average 10 - 15%

Semiconductor Fab

## Scope 3 (Upstream OPEX)

- Raw wafer (15%)\* (9%)\*\*
- Chemicals (22%)\* (4%)\*\*
- Process Gases (13%)\* (16%)\*\*
- Metals (8%)\* (24%)\*\*
- Transportation (6%)\* (16%)\*\*

## Scope 3 (upstream CAPEX)

- Process equipment (16%)\* (24%)\*\*
- Fab & equipment maintenance (6%)\*
- Fab construction (6%)\*

\*McKinsey & Company (2023): Semiconductors Practice:  
Beyond the fab: Decarbonizing Scope 3 upstream emissions

Average 35 - 40%

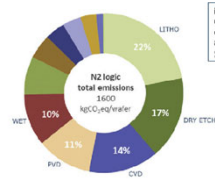
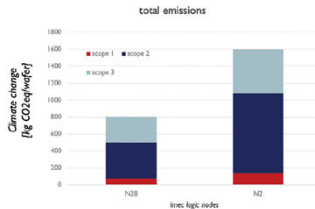
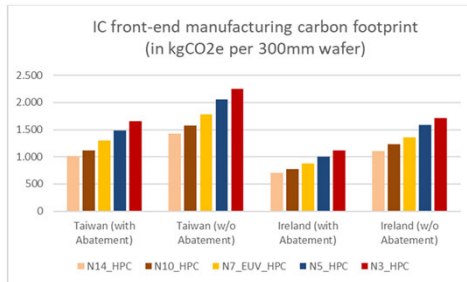
\*\*<https://www.bcg.com/publications/2023/why-chip-makers-need-to-focus-on-the-upcoming-decarbonization-challenges>

# IMEC netzero: IC manufacturing carbon footprint datasets

<https://netzero.imec-int.com/>

## Aspects influencing the IC carbon footprint:

- IC type / functionality → materials & processes
- Die size / design → wafer utilization (yield)
- Tech. node → number & types of process steps
- Process yield → defects due to complexity, etc.
- Location → energy mix (fab / equipment age)
- Market demand → fab utilization



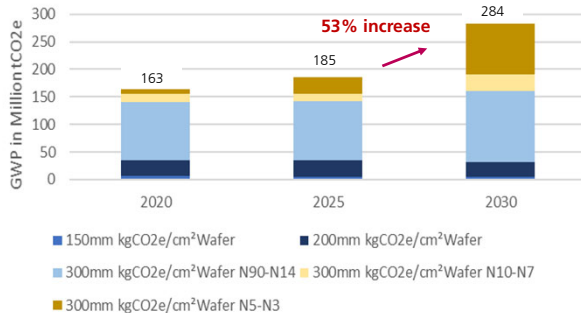
input parameters  
technology: N2  
electricity mix: 0.509 kgCO<sub>2</sub>/kWh  
abatement: up to 100%  
yield, die size, tool utilization, ...

IMEC netzero  
v1.1.0 2023-04-04 © imec

# Carbon Footprint of Semiconductor Production (Forecast)

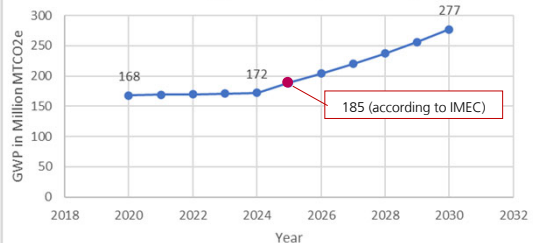
The carbon footprint of global semiconductor manufacturing is expected to increase by 53%

Carbon footprint of global semiconductor manufacturing  
(forecast by Fraunhofer IZM)



Calculation by IZM based on data from semiconductor industry environmental reports

Carbon Footprint of global Semiconductor Manufacturing (Forecast by TechnInsight)



<https://library.techinsights.com/public/hg-asset/1a965735-48b8-43a0-8ebd-7b5b8f048db5>

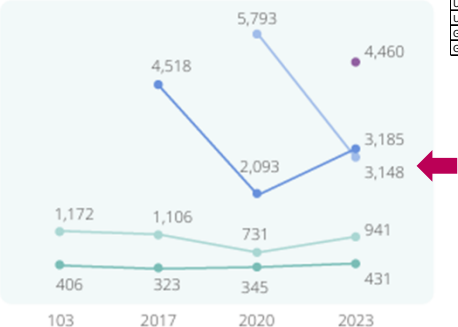
<https://www.semiconductor-digest.com/how-can-we-reduce-environmental-impact-in-chip-manufacturing/>

# TSMC reported IC manufacturing carbon footprint indicate reality

TSMC sustainability report 2024

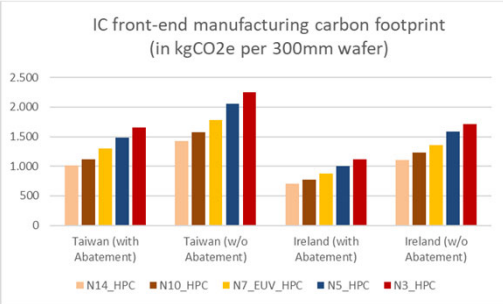
## TSMC Product Carbon Footprint

Unit: Kg CO<sub>2</sub>e / Wafer



● 8-inch wafer average ● N16~N90 wafer  
● N7~N10 wafer ● N5 wafer ● N3 wafer

Enterprise	item	unit	2021	2021	2022	2022	2023	2023	2024	2024
TSMC	wafer shipment	12" eq	14.178.630	1,05	15.252.882	0,98	12.002.177	0,73	12.910.000	0,76
TSMC	capacity	12" eq	13.500.000	1,00	15.500.000	1,00	16.500.000	1,00	17.000.000	1,00
UMC	wafer shipment	12" eq	4.391.111	1,05	4.484.000	1,01	3.202.000	0,69		
UMC	capacity	12" eq	4.201.333	1,00	4.458.000	1,00	4.674.000	1,00		1,00
GF	wafer shipment	12" eq	2.374.000	1,06	2.472.000	1,01	2.211.000	0,81		
GF	capacity	12" eq	2.239.623	1,00	2.447.525	1,00	2.729.630	1,00		1,00

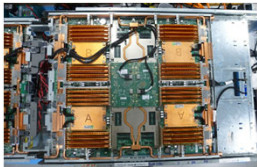


Data from IMEC: <https://netzero.imec-int.com/>

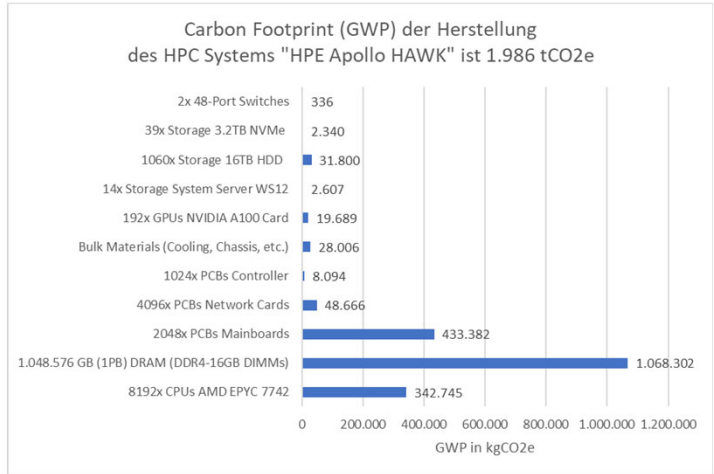
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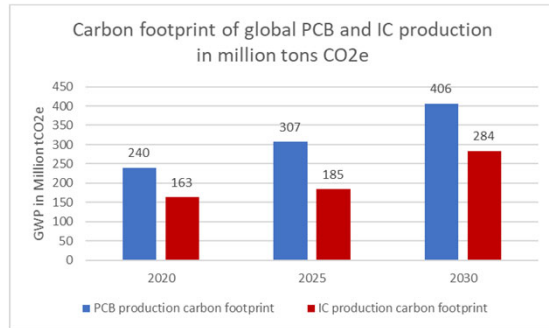
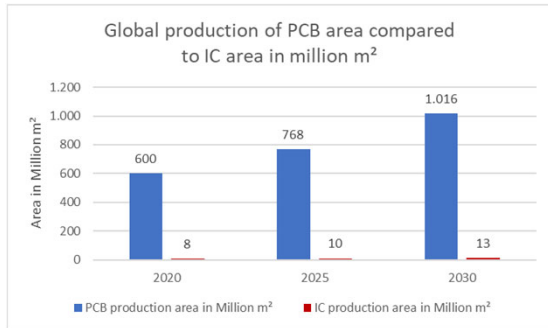
PCB →



<https://www.hrls.de/de/loesungen/systeme/hpe-apollo-hawk>

# The environmental impact of PCB manufacturing in comparison to IC

PCB design & production should also become a stronger focus of environmental improvement



<https://www.ugpcb.com/de/news/trade-news/pcb-industry-explosion-2025-global-100b-pcb-market-deep-dive-technology-breakthrough-paths/>

<https://www.precedenceresearch.com/printed-circuit-board-market>

<https://www.kingfordpcb.com/industry-news/5930.html>

# Ratio of manufacturing and use phase carbon footprint of AI compute system

Exemplary calculations based on averaged values

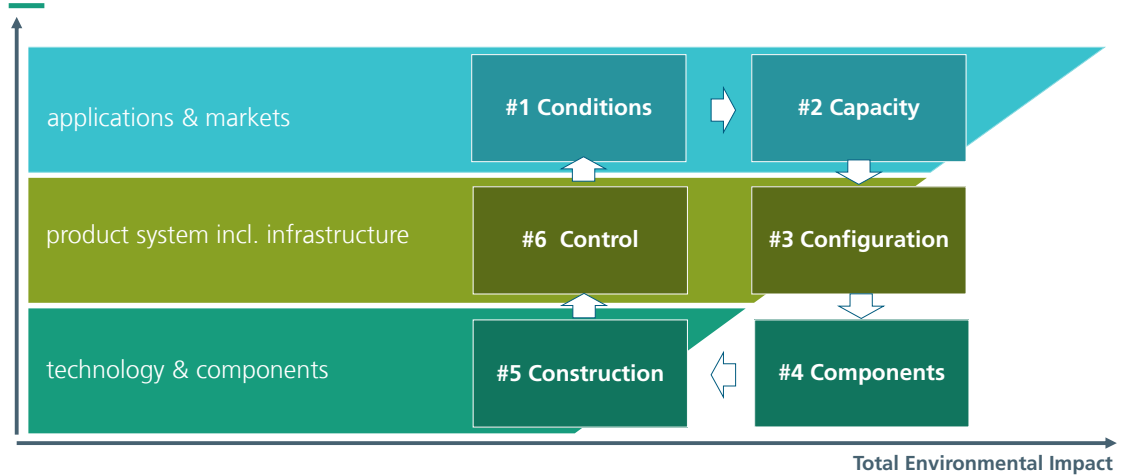
AI/HPC data center rate power:	1 Gigawatt
Power Usage Effectiveness:	1.3 PUE
Power per compute unit:	770 W
Number of compute units:	100.000 units (@15,000 Euro/unit = 1,500 Million Euro)
Manufacturing CFP:	150,000 tCO <sub>2</sub> eq (total compute units)
5 year use phase power consumption:	3.4 TWh (@ 0.25 Euro/kWh = 850 Million Euro)
• Average energy mix 380gCO <sub>2</sub> e/kWh:	1,300,000 tCO <sub>2</sub> e → 90% use and 10% manufacturing phase
• Green energy mix 120gCO <sub>2</sub> e/kWh:	405,000 tCO <sub>2</sub> e → 73% use and 27% manufacturing phase





# The Six Cues (6C method)

A reference model for data acquisition in support of environmental assessments and ecodesign of ICT



# ALU4CED: Aluminum based multifunctional housing for circular electronic devices

Laser direct structuring of a lacquer on aluminum carrier for creating antennas & touch buttons

- Polish-German R&D project funded by AiF CORNET program (2023 – 2025)

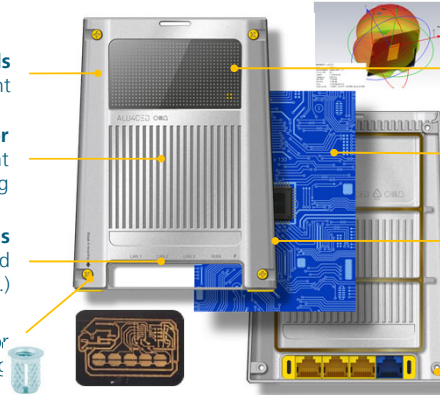


**Two identical AL housing shells**  
easy to recycle, low carbon footprint

**Aluminum housing for**  
optimizing thermal management  
and electromagnetic shielding

**Capacitive touch buttons**  
with light indicators integrated  
on outer surface (LDS techn.)

**Break-out screws** for  
fastening and ease of recycling



**Antennas** integrated on outer  
surface (LDS of lacquer technology)

**High production yield** design  
of the printed circuit board (PCB)  
with lower carbon footprint

**Anodized surface** treatment  
for personalization and appeal

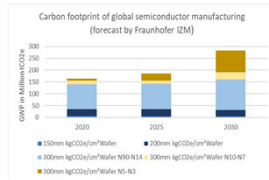
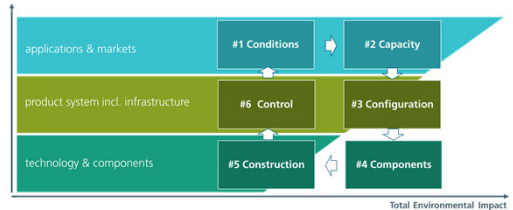
**Compact connector area** for  
easy access

# Fraunhofer IZM – Sustainable Electronics

Competencies, Methods, Tools

## We are offering competence with respect to:

- the quantification of environmental impacts of advanced microelectronics and ICT systems (IC, package, PCB, etc.)
- the estimation of environmental impacts and costs with respect to new technologies and manufacturing options based on limited data
- the analysis of microelectronic system in order to identify eco-improvement options (development of eco-design strategy)
- the support of product eco-design with focus on energy and material efficiency including design for repair and recycling (circular economy)



# Thank you for your attention

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