Fraunhofer IZM

Fraunhofer Institute for Reliability and Microintegration IZM

Electronic Packaging Days 2025

Dr. Tolga Tekin

Photonics for AI Data Centers

Bottleneck

Off - Chip/Chiplet/Core Interconnects

A key bottleneck to the realization of next generation systems for all identified high performing applications/industries (where **big-, secure-data** is in) including System-in-Package and System-on-Chip, is the lack of **off-chip/chiplet/core interconnects** with

- **low-latency,**
- **high-bandwidth,**
- **and high density.**

The objective is to develop a **CMOS compatible underlying technology** to enable next generation photonic layer within the 3D SiPs/SoCs towards converged microsystems.

Packaging for Photonics

ITRS International Technology Roadmap for Semiconductors

2007 EDITION

ASSEMBLY AND PACKAGING

Packaging for Specialized functions
Optoelectronic Packaging
RF and Millimeter Wave Packaging
Medical and Bio Chip Packaging
MEMS Device Packaging
Electronics in Textiles and Wearable Electronics
Automotives Electronics
Solar Cell Packaging
Advanced Packaging Elements

IEEE JOURNAL OF SELECTED TOPICS IN QUANTUM ELECTRONICS, VOL. 17, NO. 3, MAY/JUNE 2011

Review of Packaging of Optoelectronic, Photonic, and MEMS Components

Tolga Tekin, *Member, IEEE*

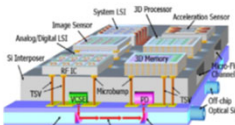


Fig. 33. Conceptual structure of 3-D heterogeneous optoelectronic integrated SOS for intelligent vehicle system with variable signal-processing function depending on moving speed [112].

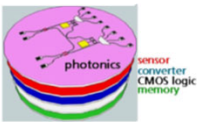


Fig. 34. Extended 3-D integration, CMOS-compatible 3-D SiP integration with photonics layer. "New SiP technology using a high-bandwidth photonic interconnection layer for converged microsystems-PICSiP" [117].

Photonics for Packaging

HIR
HETEROGENEOUS INTEGRATION ROADMAP

2023 Edition Chapter 9: Integrated Photonics

2021 Edition Chapter 2: High Performance Computing and Data Centers
Chapter 8: Single Chip and Multi Chip Integration
Chapter 16: Emerging Research Devices
Chapter 21: SiP and Module System Integration
Chapter 13: Co-Design for Heterogeneous Integration

Silicon Photonics Co-Package Integration

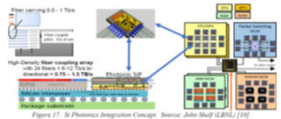


Figure 17. Si Photonics Integration Concept. Source: John Shalf (LBNL) [10].

Fraunhofer IZM

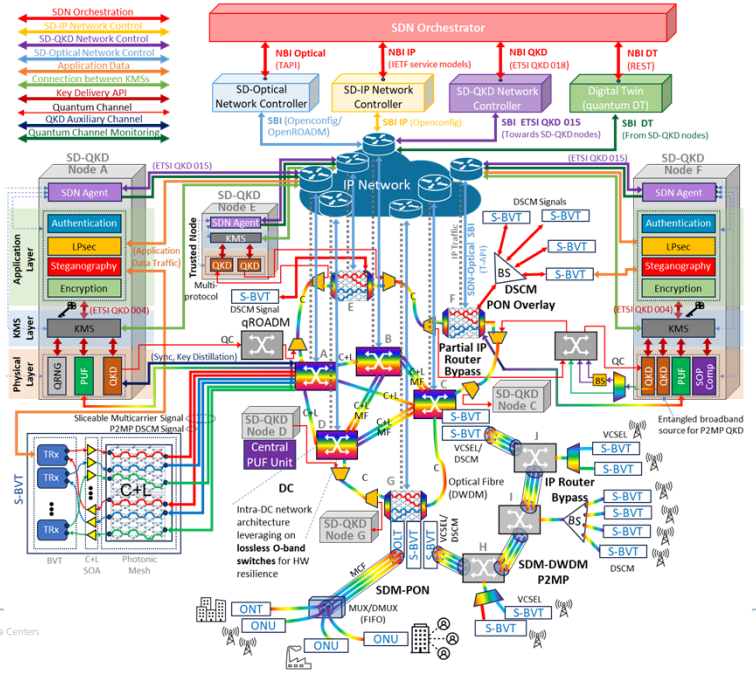
2023-2026

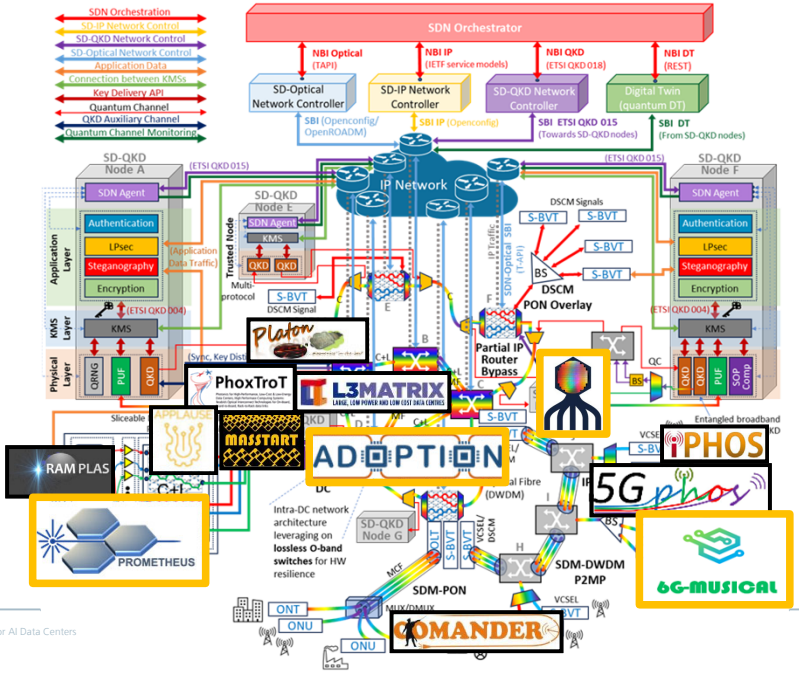
AGILE
ULTRA LOW ENERGY
AND
SECURE NETWORKS

Network softwarization and AI-based control

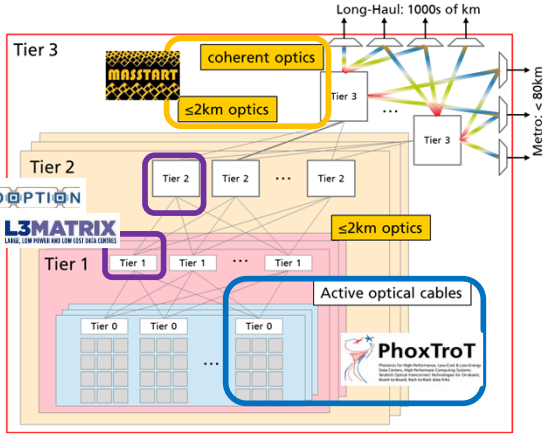
Secure data plane

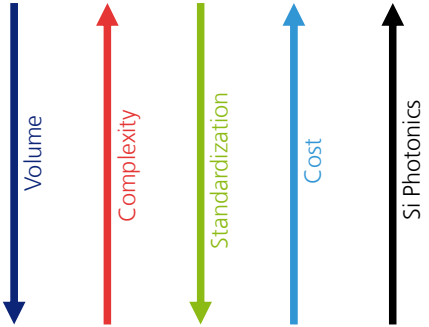
6G-ready optical transport infrastructure





AI Data Center Architecture Metrics





Tier 0 switches service a rack
Tier 1 switches service a „row" (of racks)
Tier 2 switches service a „Co-location"

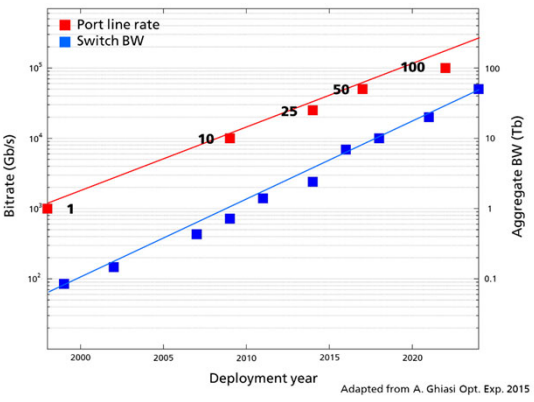
Tier 3 switches service a data-center
- Interface to long-haul network
- Also interface to metro network

Source: Benjamin Wohlfeil, Adtran

AI Data Center
Why Co-Packaged Optics?

SerDes Speed

Packaging constraints limit chip radix to 256 ports/ASIC



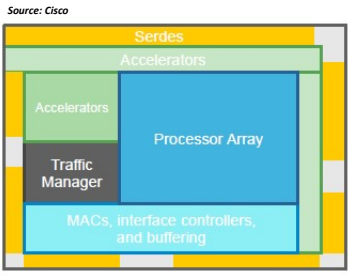
Solution is a continuous increase in bitrate:

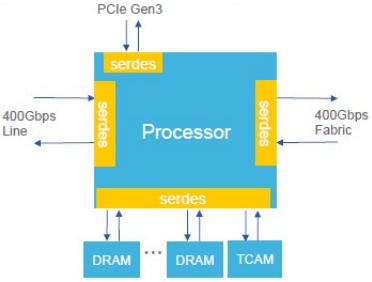
- 2023 - 51.2T switch with 256 200G ports (or 512 100G ports)
- 2025 - 102.4T switch with 512 200G ports
- 2027 - 204.8T switch with 512 400G ports

The SerDes arrays are constantly evolving to support higher bitrate.

However, SerDes power consumption increases with bitrate

100G SerDes Power Consumption





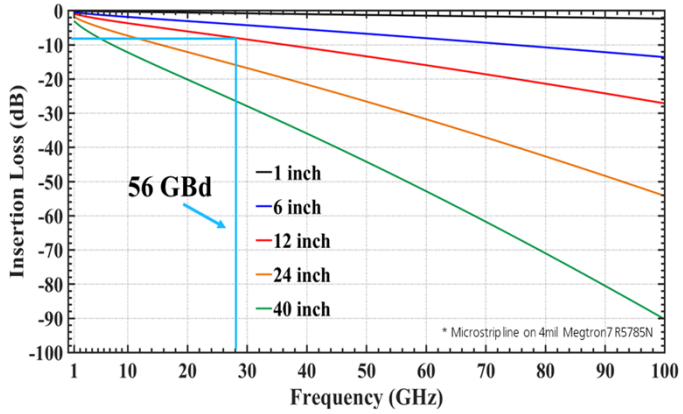
- Power consumption is 700mW for a 100G SerDes (using 7nm CMOS)
- With 256 ports, the chip I/O power consumption is: **180W**

- A **25T** switch ASIC power budget is 600W; **about 1/3 is allocated for chip I/O**

Reducing the chip I/O power and area are thus required to enable further network scaling.

Link Budget

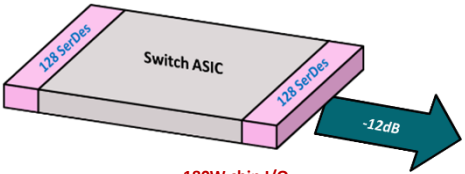
Propagation of RF signals on board material

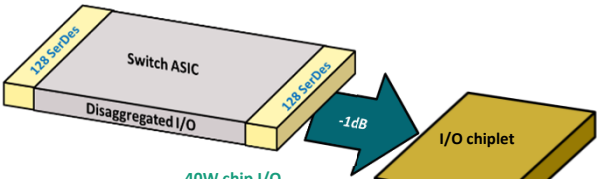


- Board material design is advancing to support the high SerDes speed and minimize the power consumption from retimers
- At 112G (56GBd), the trace loss is **8-12dB** for a 12” trace
- Transceiver power @112G is 10-12W
- Several 10k’s in data center with **2MW** power dissipation

Decoupling Logic and I/O

High Ethernet switch radix is an enabler for large scale data center networks





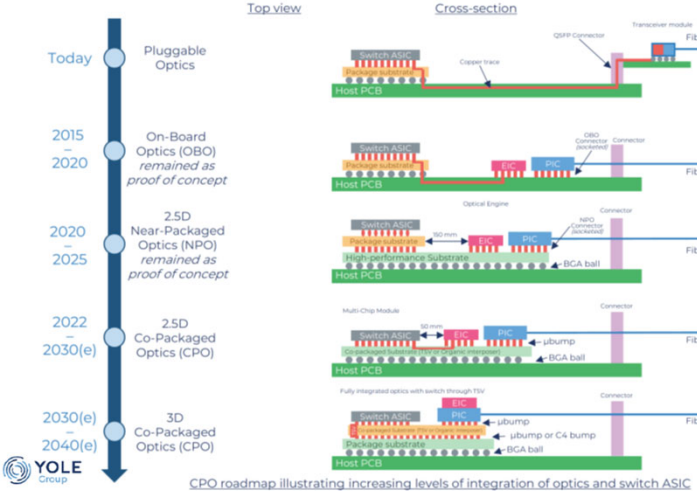
- Reduces power consumption
- The SerDes reach drops from MR/LR to USR
- The SerDes array size can be doubled with dense L/S

Source: Kobi Hasharoni, L3MATRIX

What are the crucial aspects of co-integration?

The Evolution of Co-Packaging Technologies in DC

Chip I/O disaggregation trends / crucial aspects to be considered



CPO roadmap illustrating increasing levels of integration of optics and switch ASIC

- Integration strategy (2.5D, 3D,..)
- Chip or chiplet selection (laser hybrid, heterogenous,)
- Interconnect technology (fiber-chip coupling, connectors, ..)
- Thermal management
- Power delivery and management
- Signal integrity
- System-level testing and validation
- Scalability and modularity
- Cost considerations
- Standards and interoperability

Integration of Laser for CPO

On-chip, off-chip

Hybrid Integration

Pros

Existing CM infrastructure
Moderate coupling loss
Less scalable compare to heterogenous
Efficient native InP laser

Cons

Close to ASIC: higher Tj
Not serviceable

Heterogenous Integration

Pros

Wafer-scale integration
Lowest optical loss

Cons

No optical isolator
Close to ASIC: higher Tj
Not serviceable
High R&D investment

External Laser

Image sources: Broadcom

Pros

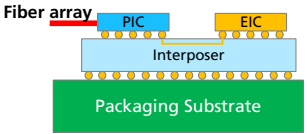
Existing CM infrastructure
Efficient native InP laser
Low Tj, higher split ratio
Reliable, repairable

Cons

Higher optical loss
Limited scalability

Integration of Silicon Photonics IC and Electronic IC

2.5D Integration



Pros

Higher density compare 2D
Trade-off scalability / flexibility
KGD

Cons

EMI, signal integrity
Design of interposer

Monolithic Integration

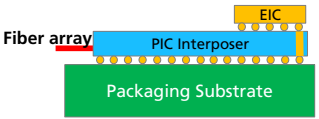
Pros

Better EMI, signal integrity
packaging steps

Cons

BW density
Cost
Thermal crosstalk

3D Integration



Pros

Density
WDM scalable

Cons

TSV on PIC
Yield

Energy efficiency

Source: Keren Bergman, Columbia University

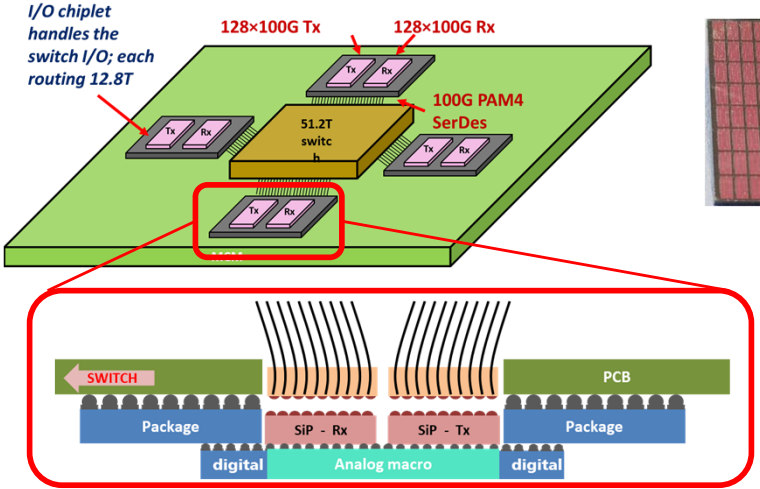
Fraunhofer IZM

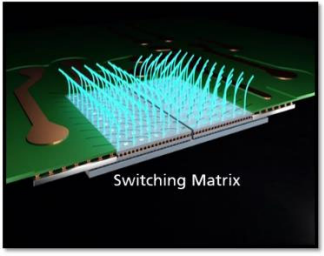
Photonics Co-Packaging R&D Efforts

L3MATRIX

2D Silicon Photonics Tx and Rx matrices to handle traffic

2015-2019

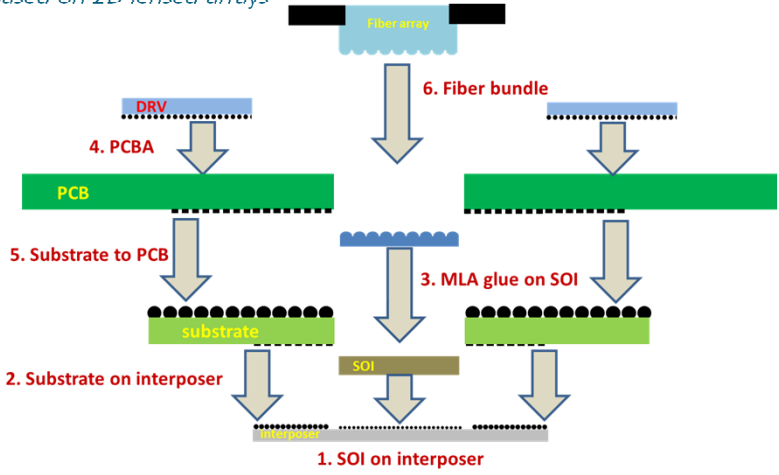




Large Scale Silicon Photonics Matrix for Low Power and Low-Cost DCs

Assembly flow based on 2D lensed arrays

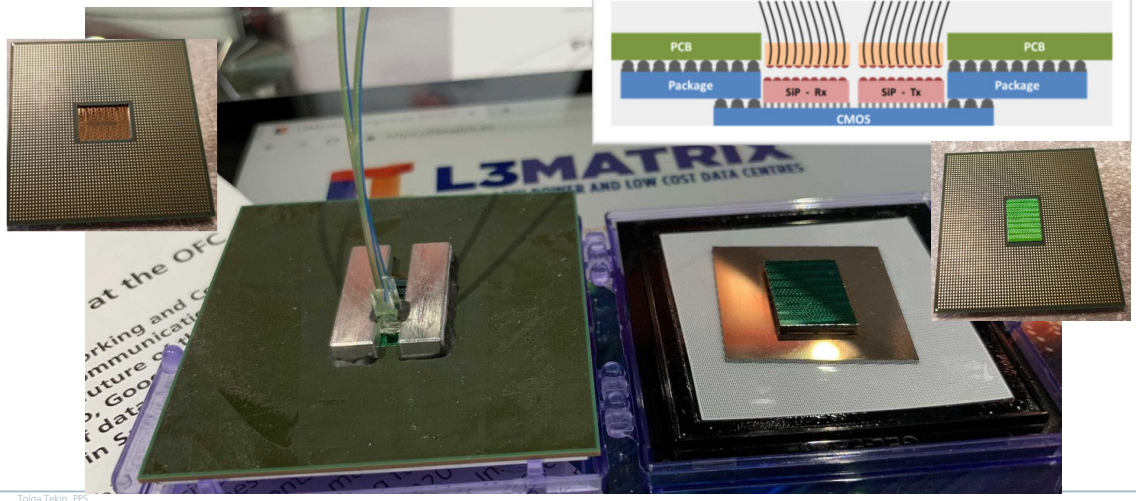
2015-2019



Large Scale Silicon Photonics Matrix for Low Power and Low-Cost DCs

Matrix vertical fiber coupling

2015-2019



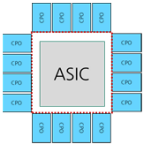
ADOPTION

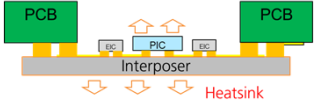
Next Generation: 204.8Tb/s switches for AI data center

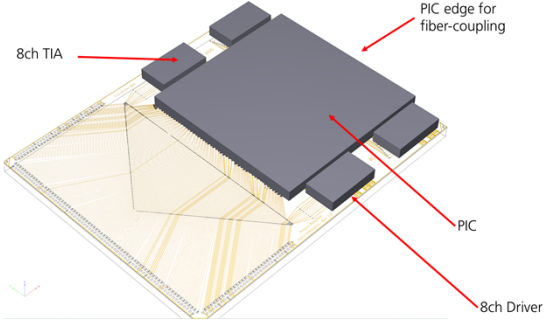
ADOPTION

2023-2026

- Silicon interposer 32ch PIC 112Gb/s/ch
- Create a European **ecosystem**/value chain around **CPO** from chip fabrication, to advanced assembly, **system integration** and the deployment by cloud computing operators.
- Low power (**3pJ/bit**), low cost (**<0.5€/Gb/s**) switching solutions for intra-data center networks targeting beyond **204.8Tb/s** switches and an increased switch radix.







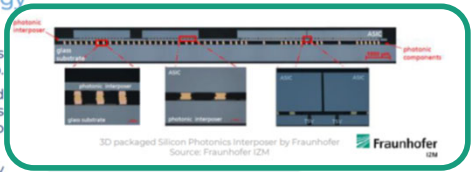
Fraunhofer IZM

What is the enabling technology for co-packaging?

PHOTONIC INTERPOSER

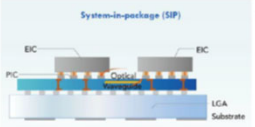
Enabling CPO through 3D packaging technology

- Photonic or "Optical" Interposer with integrated silicon photonics merges photonic and electronic functionalities within a single chip.
- Due to technology node disparity between Electronic Integrated Circuit (EIC) and Photonic Integrated Circuit (PIC), heterogenous integration technology is used to integrate PIC and EIC to minimize minimum coupling losses.
- 3D bonding technology scaling has correlated in energy efficiency scaling and lower parasitic capacitance at the EIC/PIC interface as shown by IMEC.
- PIC can also act as an active interposer and integrate multiple EICs as demonstrated by Lightelligence. The data is transmitted between EICs using waveguides and used in their Hummingbird™ system.



3D packaged Silicon Photonics Interposer by Fraunhofer
Source: Fraunhofer IZM

Fraunhofer IZM

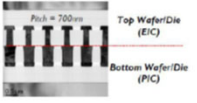


Optical Network on Chip where PIC is an active interposer to transmit data between EICs using waveguides.

Source: Lightelligence

LIGHTELLIGENCE

	Scaled pbumps (WLUF)	Embedded pbumps	Die-to-Wafer Hybrid Bonding	Wafer-to-Wafer Hybrid bonding
Pitch	50µm → 20µm	40µm → 5µm (3µm)	20µm → 3µm (2µm)	3µm → 0.5µm (0.4µm)
Die-to-die gap	12µm	4µm	~0µm	~0µm
Cross-section				
Interface parasitic Capacitance	~60fF → ~15fF	~40fF → ~2fF	~10fF → ~1fF	~2fF → <1fF



imec

EIC/PIC heterogeneously integrated interface as shown by IMEC. As the pitch is scaling, energy efficiency has also scaled, and the interface parasitic capacitance reduces.

Source: IMEC

YOLE Intelligence

EIC: Electronic Integrated Circuit
PIC: Photonic Integrated Circuit

Fraunhofer IZM

World's first 3D Packaged Silicon Photonics Interposer

PhoxTroT

2012-2017

2019 IEEE 69th Electronic Components and Technology Conference (ECTC)

3D Silicon Photonics Interposer for Tb/s Optical Interconnects in Data Centers with double-side assembled active components and integrated optical and electrical Through Silicon Via on SOI

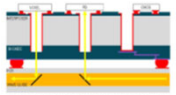
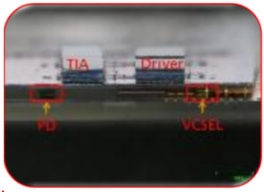
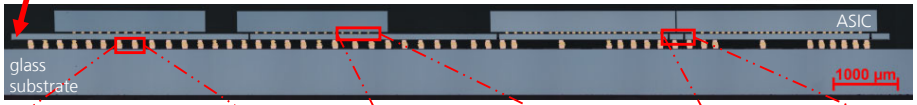
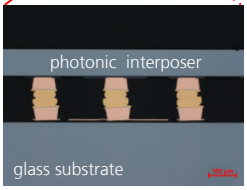


Figure 1: Interposer with optical TSVs for the transmittance of light signals from the PIC to the PCB (left) and vice versa (middle) and an electrical TSV (right)

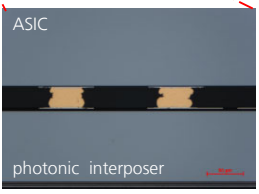


photonic interposer

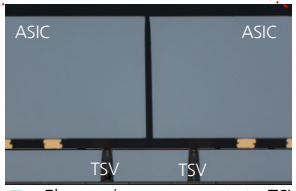




- WG-Side to substrate
- Optical components to WG-side
- Optical connection between optical components & interposer



- Electronic components to TSV-side



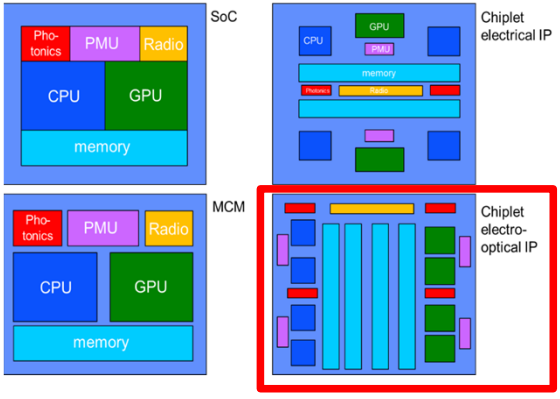
- Electronic components to TSV-side
- TSV-side to WG-side (TSVs)

Fraunhofer IZM

Beyond CPO?

Photonics Co-Packaging → Photonics Chiplets

An enabling tool to expand the ecosystem



- *SoC: single chip solution*
- *MCM: Disaggregation into functional blocks and placing on a multichip module*

Chiplet:

- Overall system performance
- Optimum production cost
- Minimize risk and reduce time to market

Package level:

- Photonics network between chiplets. The bandwidth and the energy efficiency can be increased compared to current CMOS solutions.

An additional layer to be included in the redistribution layer!

Photonics layer as part of RDL

Packaging for Photonics → Photonics for Packaging

Proven semiconductor technology

Adoption by industry volume leaders

Innovation in material, design, equipment, automation, EDA

Collaboration of communities :

Photonics – Semiconductors – Packaging