Fraunhofer IZM

Fraunhofer Institute for Reliability and Microintegration IZM

Electronic Packaging Days 2025

Hermann Oppermann

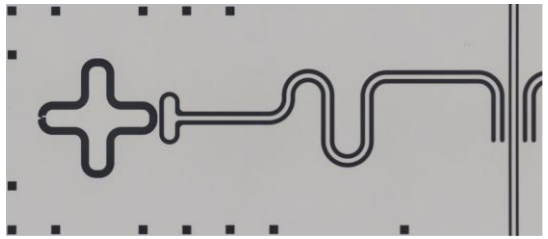
Tailoring Packaging for Advanced Quantum Applications

Packaging of advanced quantum applications

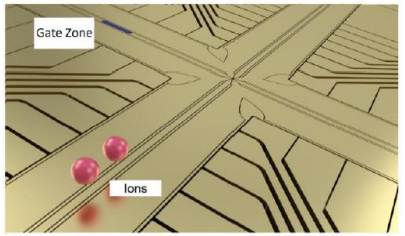
What are the challenges?

➢ **A set of technologies is required to integrate fragile quantum devices into usable, scalable systems. Such as**

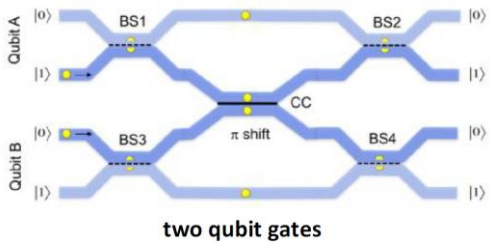
superconducting qubits



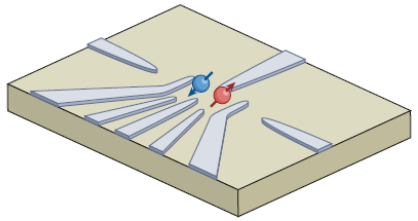
Ion traps



photonic circuits



spin-based qubits



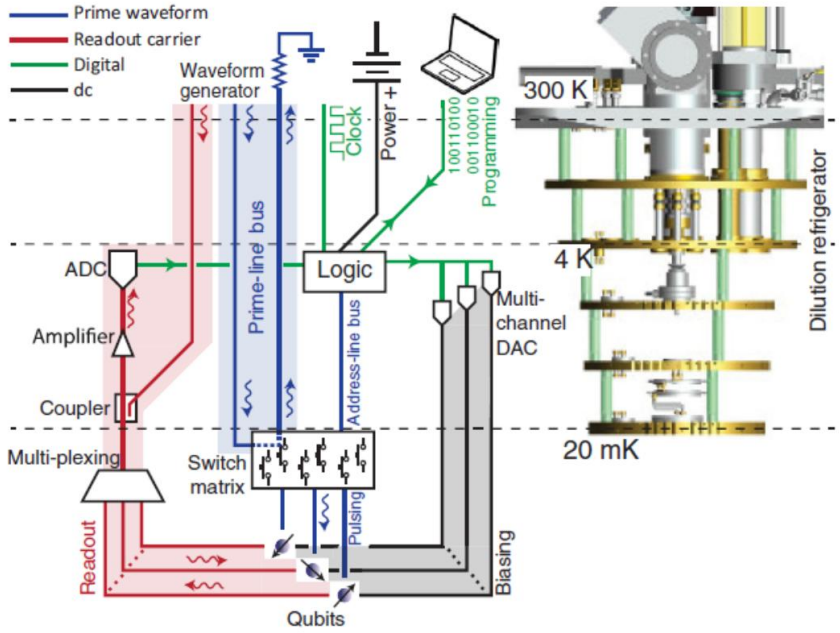
➢ **Quantum packaging faces unique challenges because quantum states are extremely sensitive to**

- **temperature**
- **electromagnetic noise**
- **vibration**
- **material defects**

Superconductive Qubit Packaging

Operating Environment and Packaging Challenges

- → Temperature: 10 to 20 mK inside a dilution refrigerator.
- → Scalability: quantum computer with thousands or millions of qubits
- → Reliability: Bump bonds, TSVs, and superconducting interconnects must be stable at cryogenic cycles
- → Integration density: Keep qubits close to each other for coupling and routing signals without crosstalk
- → Wiring bottleneck: Each qubit needs multiple microwave/control lines. Higher wiring density of superconducting qubits in cryogenics
- → Thermal load: Each extra coax line adds heat load, space, and noise. Thousands of coaxial lines won't fit into a dilution fridge.
- → Active electronics at cryo-level must be ultra-low-power (readout circuit ~1 nW (30 µA, 30 µV).
- → Cooling power is very limited: 1 W @ 4 K, but <10 µW @ 20 mK
- → Isolation: Must suppress electromagnetic interference (EMI), magnetic flux noise, and thermal photons

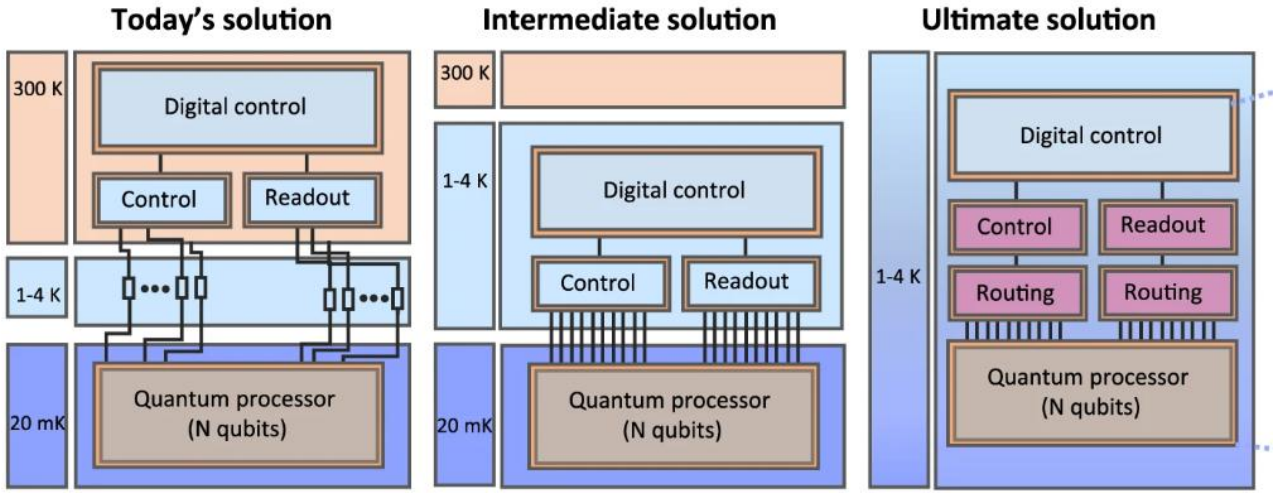


source: J. M. Hornibrook et al.: Cryogenic Control Architecture for Large-Scale Quantum Computing, PHYS. REV. APPLIED 3, 024010 (2015)

- ➢ 3D integration and flip chip bonding down to 15 µm pitch for qubits, readout and controller chips
- ➢ superconducting interposer with TSVs and multiple routing layers with low losses (microwave)
- ➢ micro-bump interconnects based on indium with temperature cycling capability at cryogenic temperature

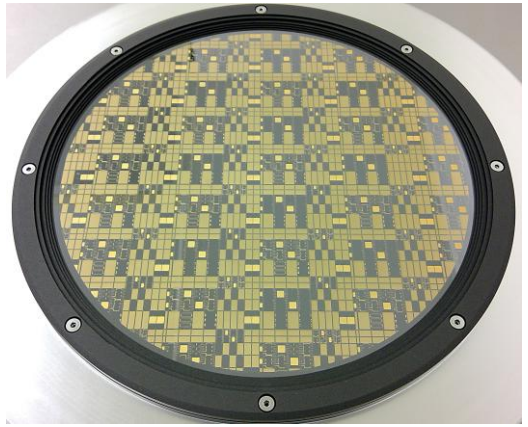
Core Functions of Superconducting Qubits

- **Thermal Management**
  - Operation at milli-Kelvin (mK) regimes for superconducting qubits
  - Minimize heat leaks between cooling stages
- **Signal Delivery & Interconnects**
  - Microwave lines: low loss, low cross-talk (superconducting routing circuits)
  - Wiring lines: ultra-low resistance to avoid heating in cryogenic environments
- **Integration with Classical Control Electronics**
  - Cryo-CMOS or superconducting electronics: Co-packaging with qubits
    → advanced packaging
  - Reduce wiring bottlenecks: moving signal processor closer to the quantum chip
    → increased I/O density

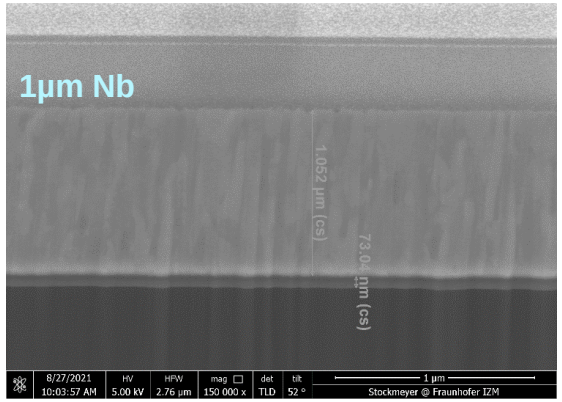


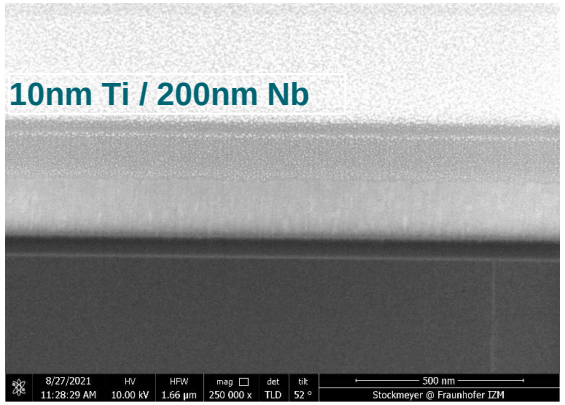
Superconducting Qubit Packaging

Superconductive Metallizations

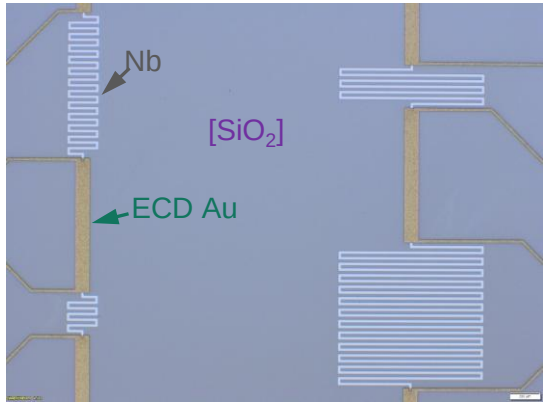


8” wafer: Nb 150nm / Au 150nm; electroplated Au: 1.5µm

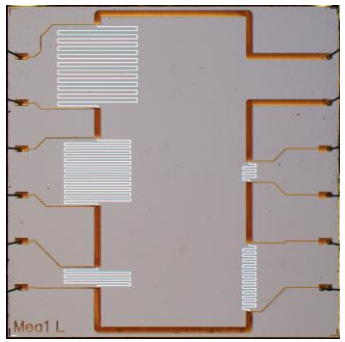


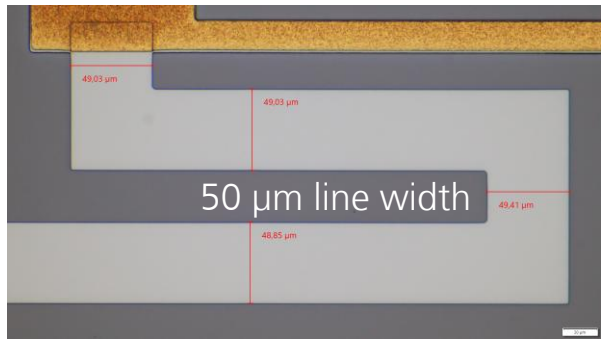


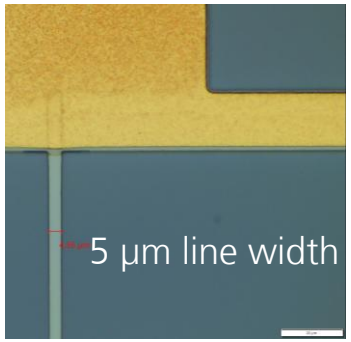
Sputter deposition of 1µm Nb, NbN, 200nm Nb and Ti / Nb



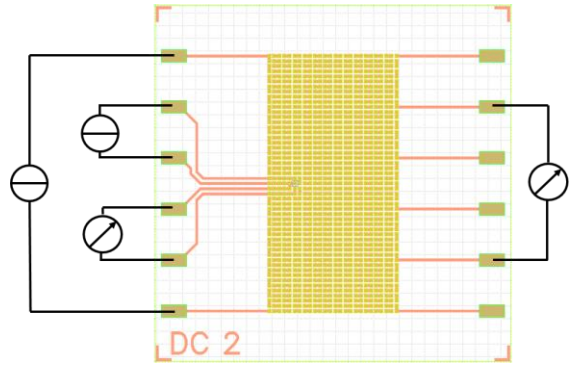
Etching of Nb; Plating of Au







Niobium patterned: 50 µm down to 5 µm line width & electroplated Au 1.5 µm



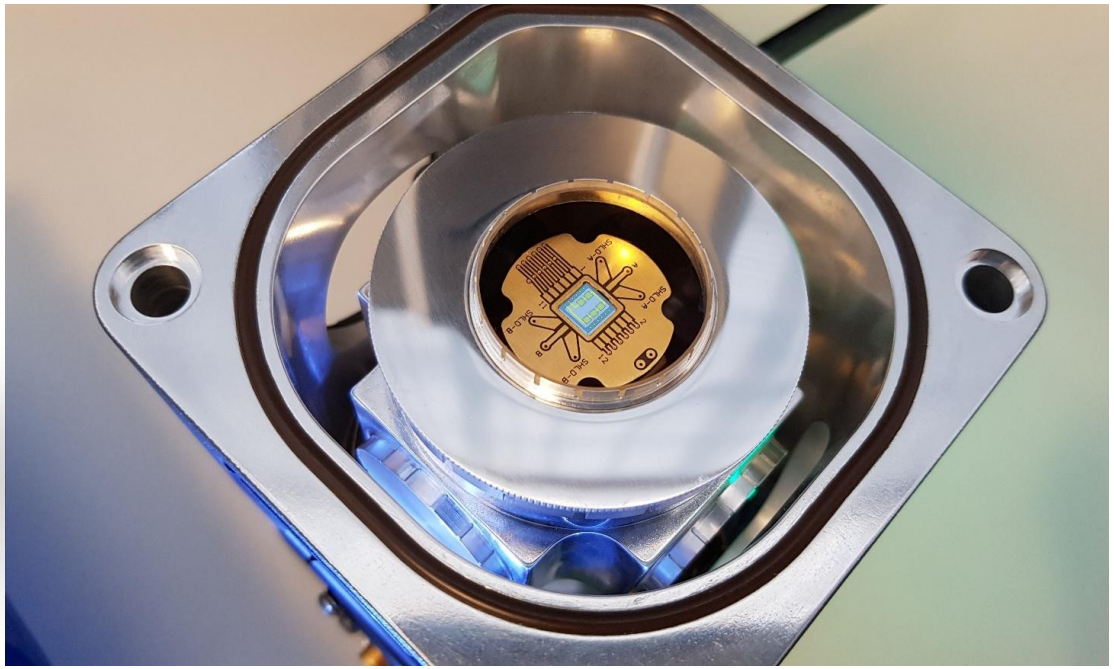
Electrical test chip:

- 5476 Bumps
- daisy-chain,
- isolation test
- 4-point-Kelvin

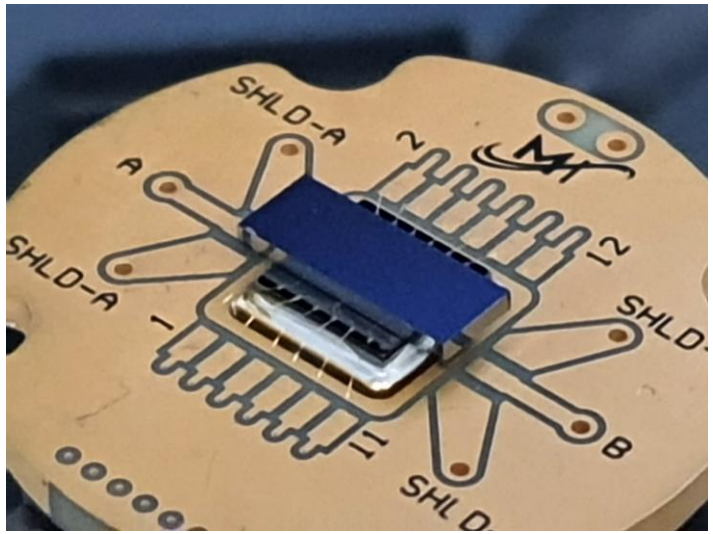
Flip chip test vehicle for Indium bumps on Nb

Superconducting Qubit Packaging

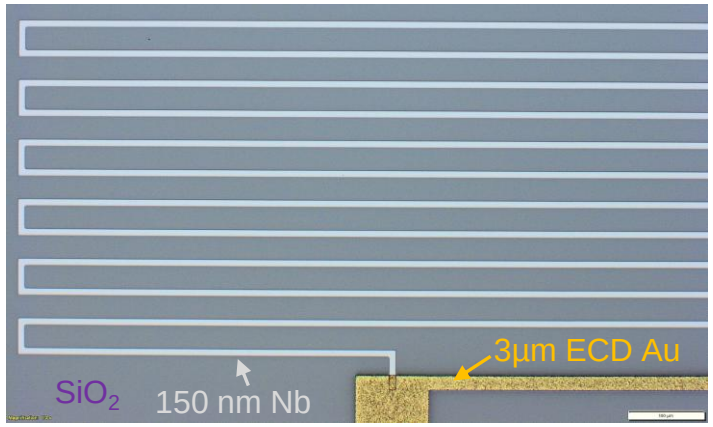
Cryogenic Testing



View on sample mount



Flip chip bonded test vehicle with indium bumps on sample mount



10 µm lines
50 µm pitch

Cryogenic Testing Capabilities:

- **Temperature ramping between 300K and 3.2 K**
- **Magnetic field application up to 0.7 T**
- **RF capability up to 20 GHz**

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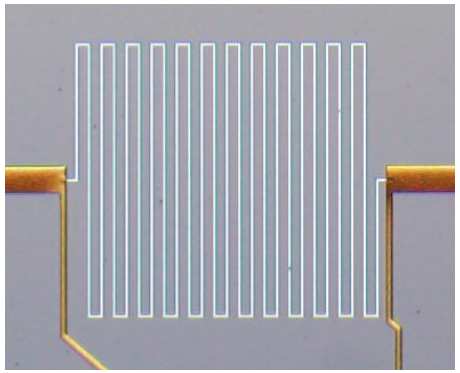
Cryogenic Integration and Interconnect Technology

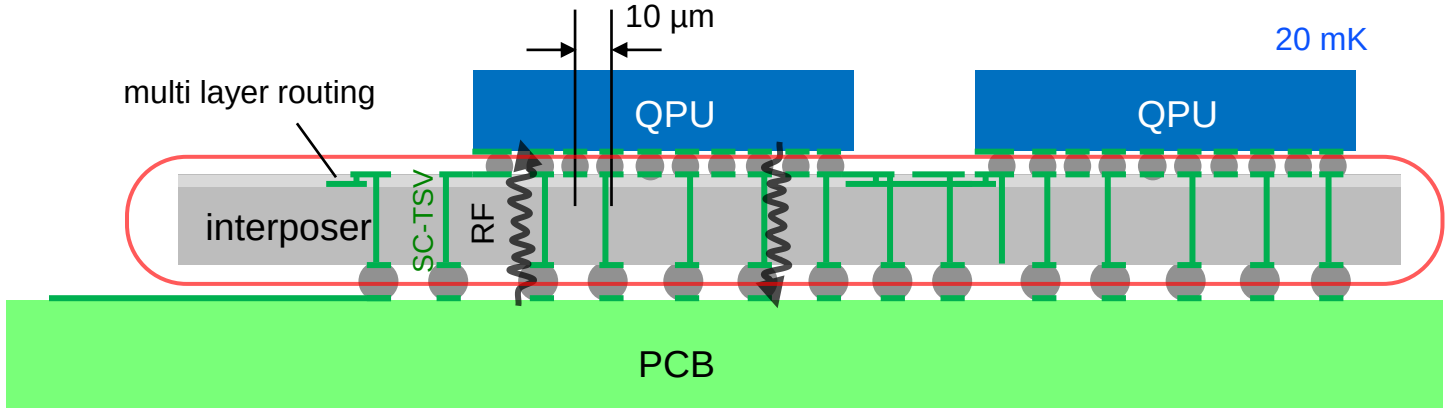
Interposer Technologie / 3D Integration

Scalability for integration of multiple QPUs

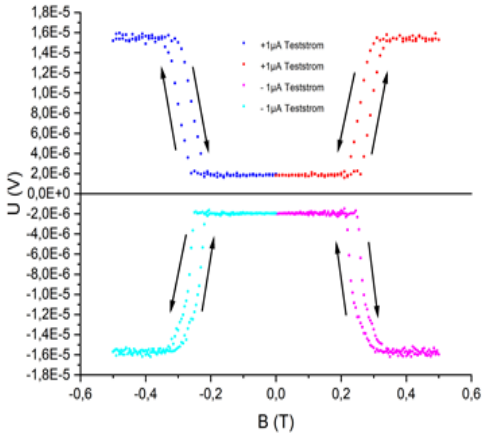
- Multilayer routing: superconductors, e.g. Nb, NbN
- Interposer with superconductive TSVs
- Low loss RF routing



Niobium 150 nm patterned



measurement of critical magnetic field strength



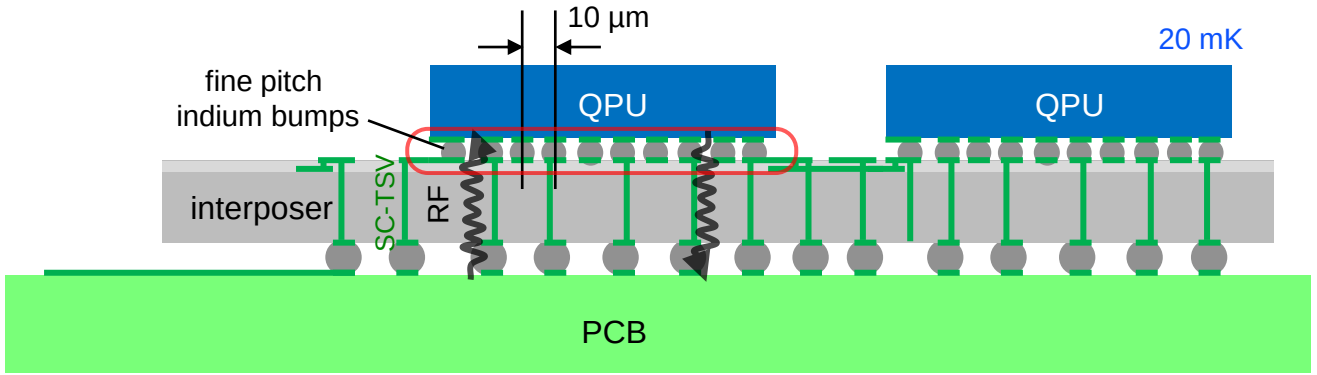
measurement of niobium with 1µA at 3.3 K

Cryogenic Integration and Interconnect Technology

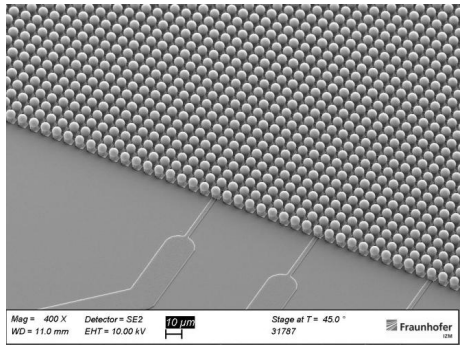
Chip Integration and Interconnect

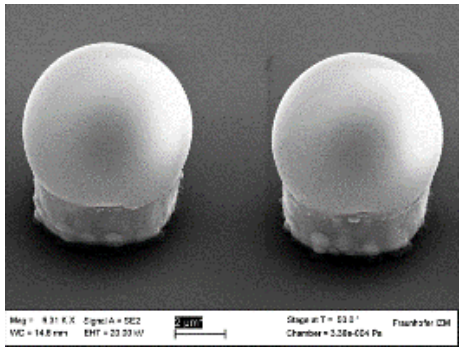
Scalability for applications with 10^5…10^6 qubits

- Extreme high interconnect density for QPU
  → <10µm bump pitch
- Indium & indium-tin: → superconducting bump interconnect
  → ductile at low temperatures

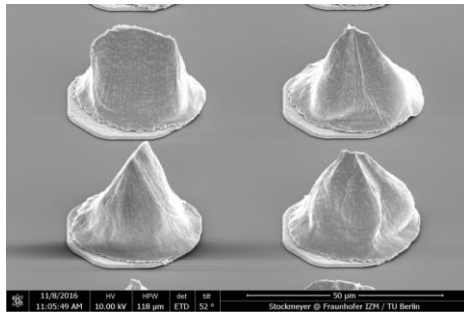


Low Temperature Bonding In-Au: 80°C
In-In: 30°C

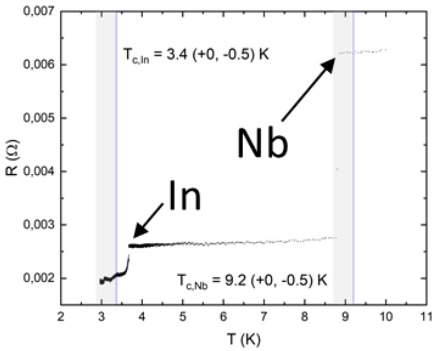




electroplated indium bumps 7.5 µm pitch
4 µm bump diameter, 3.5µm space



indium: ductile fracture mode
→ low temperature toughness



indium: critical
temperature at 3.4 K

Ion Traps Qubit Packaging

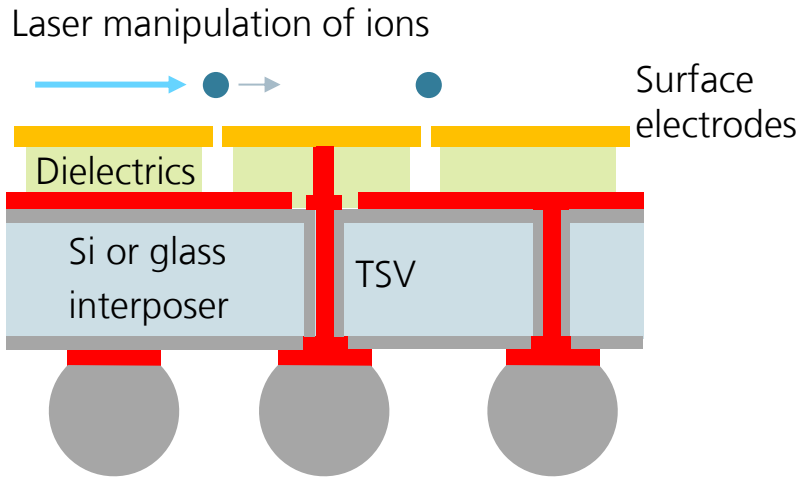
Operating Environment

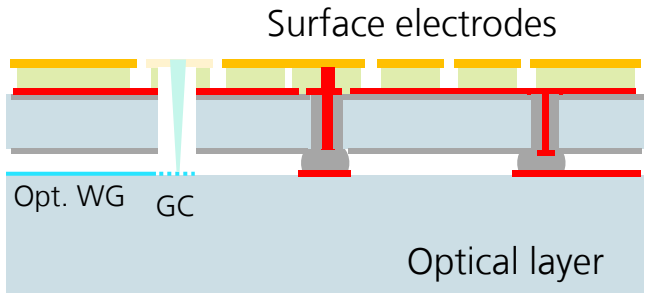
Fabrication:	**Semiconductor processes: Au or superconducting electrodes patterned on sapphire/Si. - mounted inside vacuum chambers using UHV-compatible packaging technologies - include chip carriers with UHV feedthroughs for electrical connections**
Vacuum:	**Ions are suspended in electromagnetic Paul or Penning traps. Requires UHV: ~10^{-11}–10^{-13} Torr. Prevents ions from collision with gas molecules.**
Temperature:	**Ion traps operate at room temperature, but cryogenic traps might be more stable.**
Optical access:	**Laser beams used for ion cooling, state preparation, and entangling operations. Each ion needs multiple laser beams; scaling to thousands is hard without photonic integration.**
Electrical control:	**Ions are confined by RF and DC voltages applied to electrodes on the chip. Integration with control electronics needs dense wiring without introducing noise or breaking vacuum seals.**
Magnetic field control:	**Qubits require stable magnetic fields.**
Vibration Isolation:	**Ion traps require nm-scale stability. Even slight mechanical noise can destroy precision.**

Ion Traps Qubit Packaging

Challenges in Packaging and Possible Solutions

- **Surface-Electrode Traps: with microfabrication electrodes are patterned flat on chips. They can be scaled for high volume, flip-chip packaged, and integrated with photonics.**
- **Integrated Photonics Packaging: SiN waveguides route multiple laser wavelengths directly to ion positions, eliminates bulky free-space optics and dramatically improves scalability.**
- **Cryogenic Traps: cryo temperatures improves vacuum and reduces motional heating.**
- **Compact Vacuum Modules: sealed chip packages with integrated ion source, vacuum pumping, and optical access in a few cm³ as for modular scaling.**





- **Microfabricated surface-electrode traps with TSVs**
- **Integrated photonics for scaling large number of laser beams.**
- **Hermetic sealing at chip or package level to sustain UHV environment**
- **Packaging should be suitable for cryogenic temperature**

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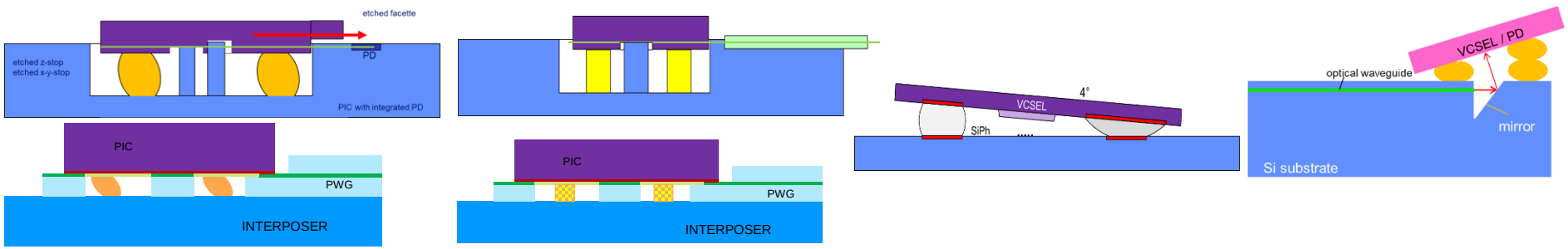
Quantum Packaging: Photonic Layer and Interconnect

Photonic Component Integration – Optoelectronics to PIC Coupling Schemes

Component	Edge emitting laser (EEL)		VCSEL / PD	
PIC interface	Butt coupling Evanescent coupling		Grating coupler Mirror	
Alignment	Solder self-alignment	TC bonding	Solder self-alignment	TC bonding
Mechanical stops	x-, y- & z-stop	z-stop	no stops	no stops
Bump interface	AuSn	Au-Au NPG-Au	AuSn SnAg	Au-Au NPG-Au



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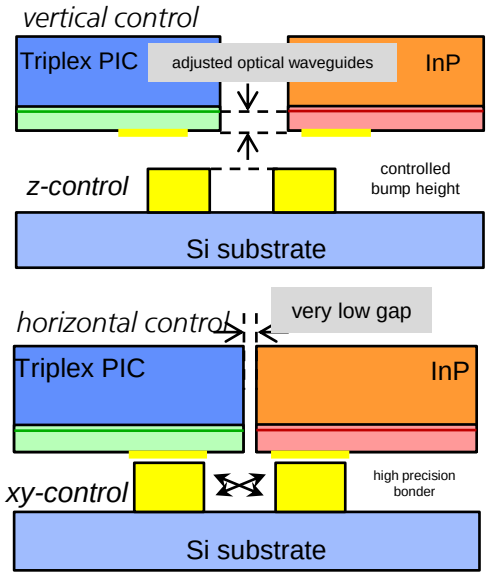
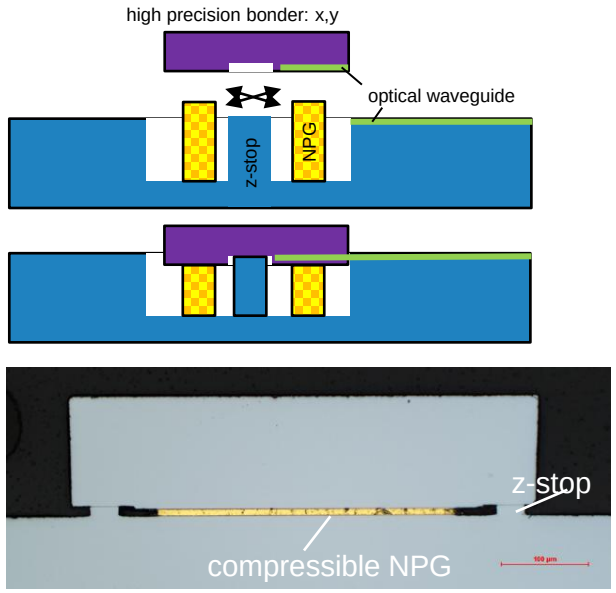
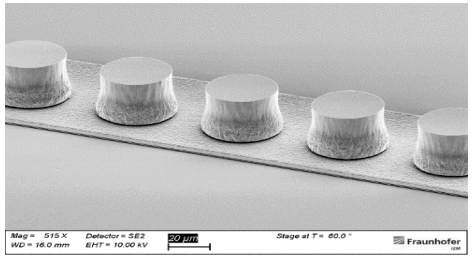
Quantum Packaging: Photonic Layer and Interconnect

Photonic Component Assembly: Passive Alignment for Optical Chip-to-Chip Coupling

High Precision Bonding using Planarized Au-Au or Nanoporous Gold (NPG)



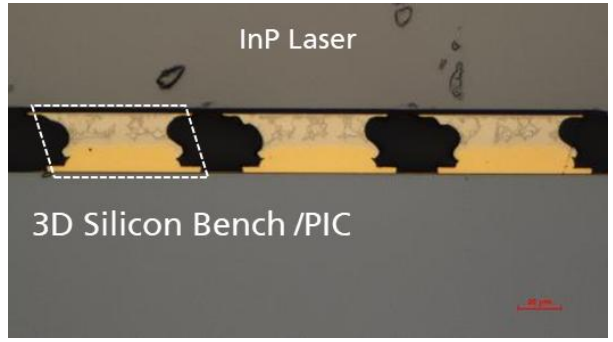


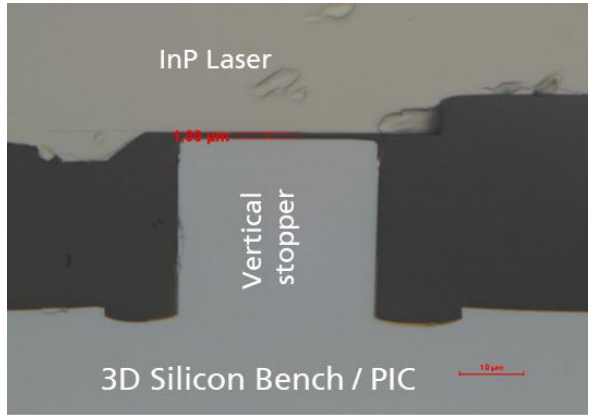


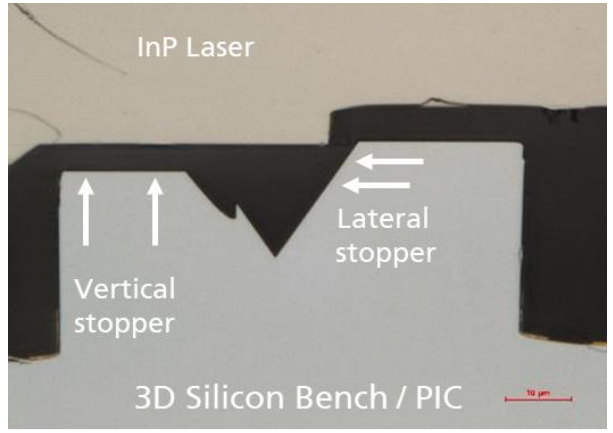
planarized Au bumps

Compressible Nanoporous gold (NPG)
- → low temperature bonding down to 150°C
- → low bonding pressure down to 15 MPa
- → low bonding time (few seconds)
- → tolerant bump planarity
- → topography acceptable

Solder Assisted Self-Alignment with Mechanical Stops using AuSn Solder Bumps







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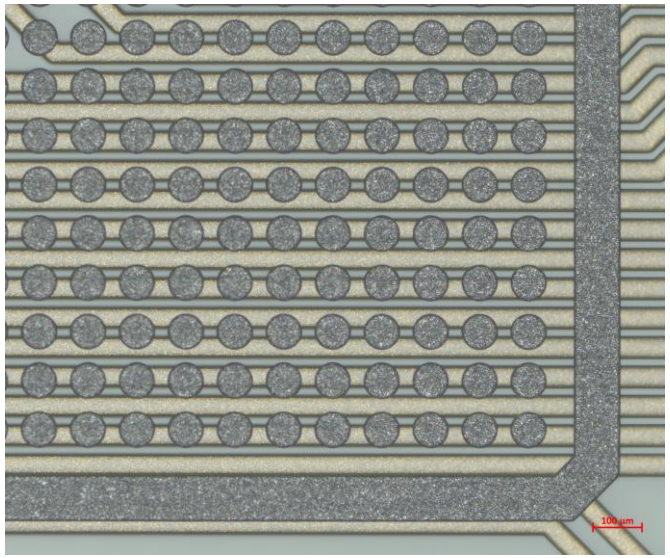
Ion Traps Qubit Packaging

Hermetic Sealing

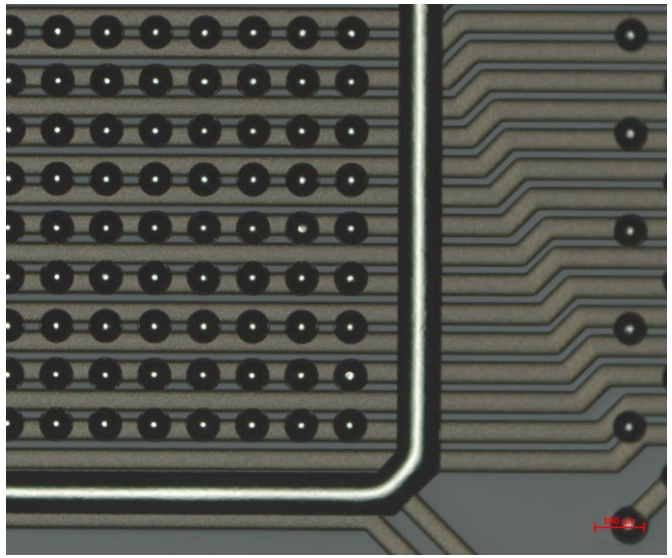
Optional: integration of getter materials

Bump array Sealing ring



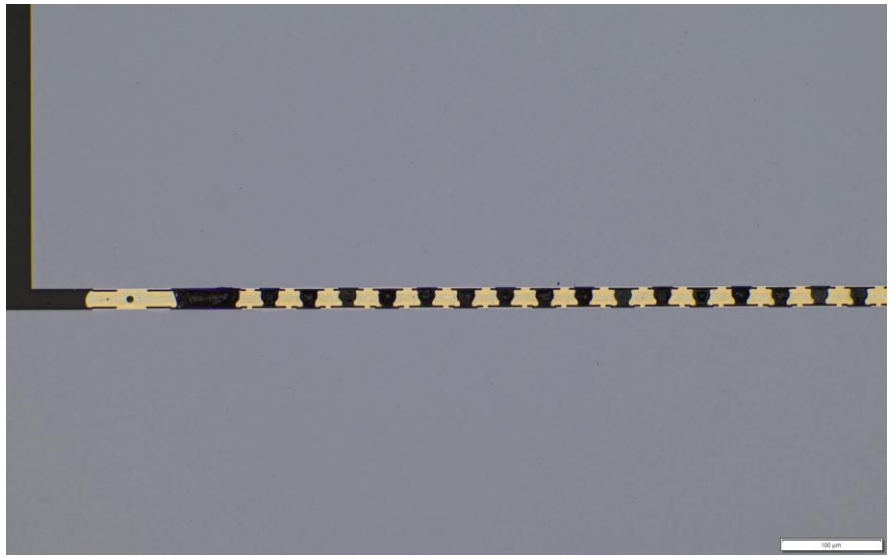
As plated

Bump array Sealing ring



After reflow

Sealing ring Bump array



After bonding

- Hermetic sealing at chip or package level to sustain UHV environment
- Encapsulation of outgassing chips or components
- Modular approach with vacuum packages for scaling

Packaging for Advanced Quantum Applications

Integration Technologies of Fraunhofer IZM

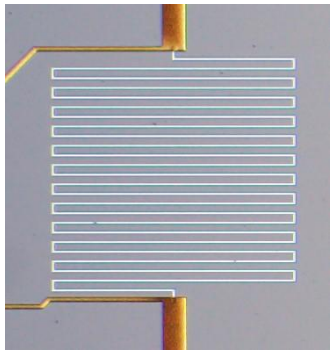
Superconducting Interposer
- Redistribution layer (Nb and NbN),
- Superconducting TSVs

Cryo FlipChip
- Bumping indium and indium-tin less than 10µm pitch
- Fine pitch flip chip bonding

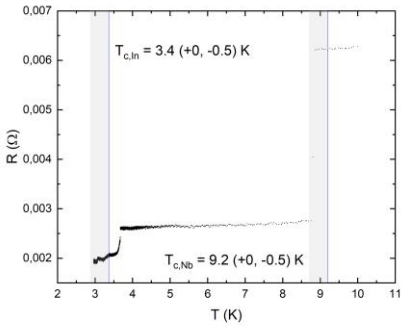
Photonics: PIC Design & Integration Technology
- Chip-to-chip optical coupling solution (butt, GC or evanescent)
- PIC integration technology to connect each qubit
  → Electrical routing on PIC wafer (RF multi-layer, TSVs)
  → Integrate mechanical stops to enhance placement accuracy

Hermetic Sealing
- Vacuum tight hermetic sealing at chip and module level

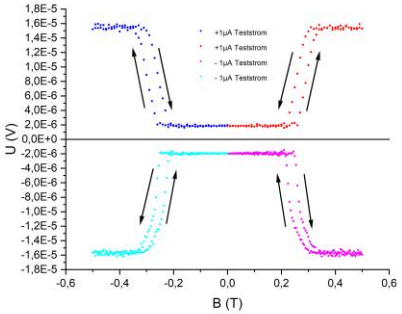
Cryogenic Test Capabilities
- Temperature ramp from 300K to 3.2 K,
- Magnetic field application up to 0.7 T
- RF capability up to 20 GHz



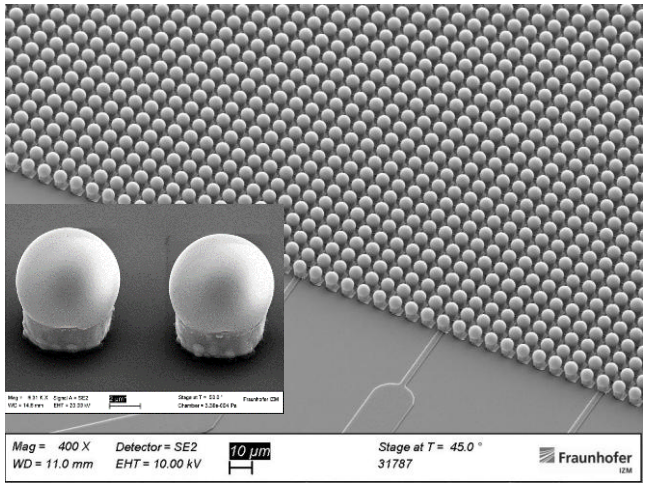
Patterned Nb lines



Test critical temperature



Test critical magnetic field



In bumps
7.5 µm pitch

Kontakt

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Thank you for your attention