

Electronic Packaging Days 2025

Karl-Friedrich Becker

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# Packaging Technology in the Digital Realm:

## Digital Twins & AI-related Tools

# Flashback to the 1980s

When chip foundries and microelectronics packaging became mainstream, digitalization was in its early days.

Today we are using a variety of digital tools to control production/logistics, to monitor process quality, to coordinate testing and to personalize products.

Actually ...

Aus: H. Völz, Elektronik für Naturwissenschaftler, Akademie-Verlag Berlin, 4. Auflage, 1986

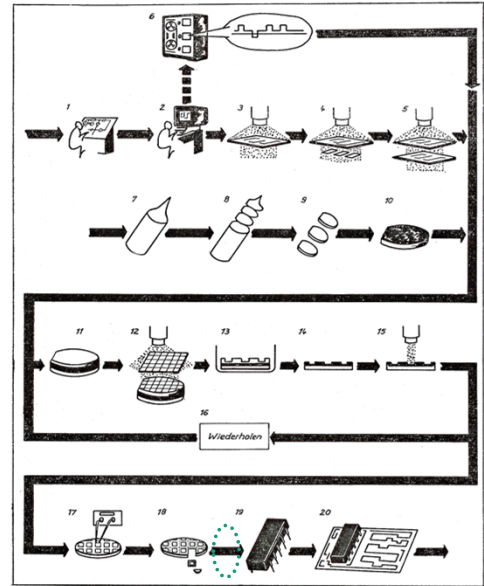


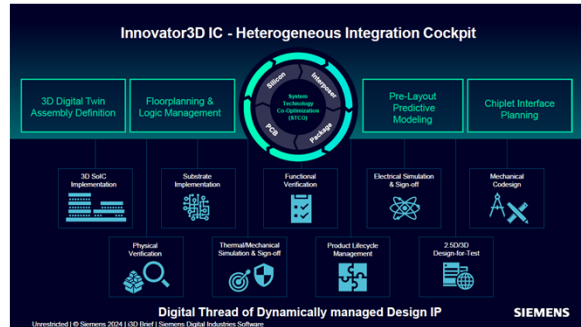
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# Today's capabilities – Frontend vs. Backend

... frontend processes are almost completely digitized.

Design tools as Cadence, Keysight, Siemens EDA, Synopsys, Zuken, ... are used to design ICs as well as systems and integrate PDK/DRC infrastructure and component simulation.

Packaging is mapped to such tools by using Assembly Design Kits [ADK], data based technology description today seen as a result of System Technology Co-Optimization [STCO].



Siemens EDA Concept for System Design / 3D Integration

# Research Landscape in 3D Heterointegration

Different Background between OSAT's and IDM's, Foundries to build 3D Modules

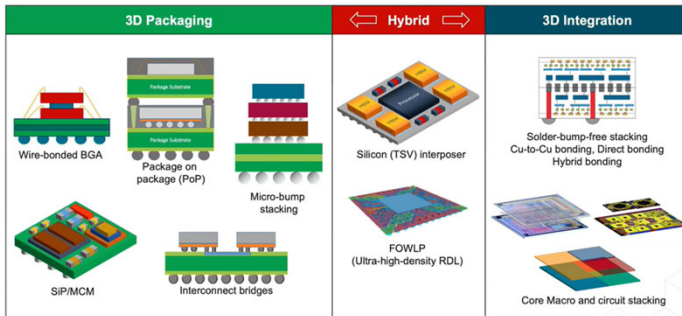
## Heterogeneous Toolbox

- **Interconnect:** Wire bond, Flip Chip, TxV, Solder Balls, Hybrid Bond, .....
- **Encapsulation:** Mold, Underfill, Paste, Glob Top, ALD, .....
- **Substrates:** Organic, Glass, Silicon, Ceramic, Leadframe, .....
- **Packaging Concepts:** 2,5D, 3D, Fan Out, Embedding, PoP, CSP, .....

Huge variety of materials

OSAT's

## 3D Packaging (Back-End 3D) vs. 3D Integration (Front-End 3D)



Source: Cadence

## Semiconductor Toolbox

- **Deposition:** Thin films of conducting, isolating or semiconducting materials.
- **Photoresist coating:** resist: positive and negative.
- **Lithography:** exposed to DUV or EUV light.
- **Etch:** remove the degraded resist.
- **Ion implantation:** tune the electrical conducting properties

Typical frontend materials

IDM, Foundry

# Digital Twins covering all phases of Product Lifetime

## Wikipedia definition:

A digital twin is a digital model of an intended or actual real-world physical product, system, or process (a physical twin) that serves as the effectively indistinguishable digital counterpart of it for practical purposes, such as simulation, integration, testing, monitoring, and maintenance

## Our working definition:

A digital twin is a digital representation of a material, component or process that you can ask questions (and you get answers!) the more sophisticated the digital twin, the more complex the questions may be.

... Digital Twins for packaging can become quite complex!

### MANUFACTURING, PACKAGING & MATERIALS

## Digital Twins For Packaging: Bridging Design, Fab, Test, And Reliability

205

19

11

103

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Packaging moves toward predictive control, but trust and validation still lag.

OCTOBER 23RD, 2025 - BY GREGORY HALEY



Digital twins dominated discussions at SEMICON West this year, appearing in keynote presentations, panel sessions, and workshops. The conversation reflected a noticeable shift in how the industry views the technology.

What once was mainly associated with design exploration now spans the manufacturing lifecycle. In packaging and assembly, digital twins are emerging as a way to connect design intent with process execution, monitor variations across multiple stages, and in some cases, prescribe corrective actions in real-time.

The pressure to virtualize packaging is mounting. Advanced integration schemes are increasing the number of variables that engineers must manage. Interconnects are tighter, materials are more diverse, and system requirements are more demanding. Even small deviations in planarity, thermal expansion, or warpage can trigger cascading failures. And while such traditional approaches as statistical process control, recipe qualification, and downstream root-cause analysis remain important, they often react too slowly to prevent yield loss once problems arise. Engineers are looking for tools that can anticipate issues earlier and provide actionable choices before damage occurs.

"Customers are demanding heterogeneous integration paths, with multiple die types in a single package," said Giel Rutten, president and CEO at Amkor. "To maintain yield and reliability, we cannot rely solely on reactive fixes. We must simulate coupling, stress, and thermal interaction up front."

### TECHNICAL PAPERS

Utilizing Chiplet-Locality For Efficient Memory Mapping In MCM GPUs (ETRI, Sungkyunkwan Univ.)

OCTOBER 30, 2025 BY TECHNICAL PAPER LINK

Performance Of A Memory System With FeRAM Vs. DRAM (Georgia Tech, Imec, NTUA)

OCTOBER 29, 2025 BY TECHNICAL PAPER LINK

AUTOSAR-Aligned Analysis Of 180 SoC Vulnerabilities In Auto Architecture (Chalmers, Univ. Of Gothenburg)

OCTOBER 29, 2025 BY TECHNICAL PAPER LINK

An Overview Of Recent Progress On The EUV + DSA Strategy (Univ. Of Chicago, Berkeley Lab, Argonne)

OCTOBER 28, 2025 BY TECHNICAL PAPER LINK

Multimodal LLM Assistant For Chip Physical Design (National Taiwan Univ., UCLA, NVIDIA)

OCTOBER 28, 2025 BY TECHNICAL PAPER LINK

### Knowledge Centers

Entities, people and technologies explored

LEARN MORE

# Reference Projects – Chiplet-Related Projects

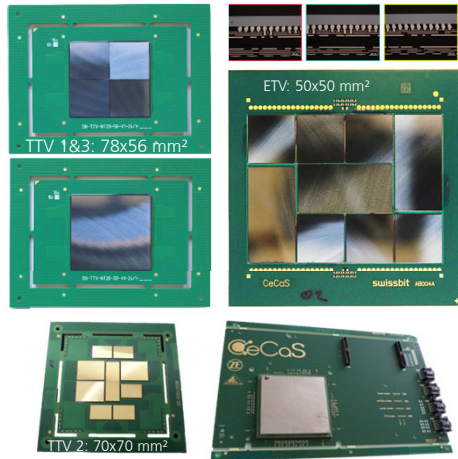
## Process Development and Data Acquisition

Small-Volume Manufacturing of Engineering Samples for an Industrial Partners – yielding valuable information on process quality and stability depending on varying boundary conditions: Die Size & Configuration, PCB Stackup, Materials

-> **Data collection towards a process model / Digital Twin**

Inside CeCaS a Lab-to-Industry Scenario was deployed -  
In cooperation between Conti (System Owner), Swissbit (Manufacturing Source) and Fraunhofer IZM (RTD); assembly feasibility was proven at IZM – data transfer to Swissbit allowed fast manufacturing setup -  
Chiplet assy on Carrier Board at Conti based on IZM/Swissbit data

-> **Data Transfer from Lab2Industry**



Chiplet Test Vehicles from CeCaS Project

# Reference Projects – Chiplet-Related Projects

## Data Depolyment towards a Reliability Digital Twin

### Material Data For Chiplet Assembly:

PCB / Underfill / Solder / Silicon / Structural Adhesive

### Process Description:

Process Steps / Equipment & Handling / Temperatures

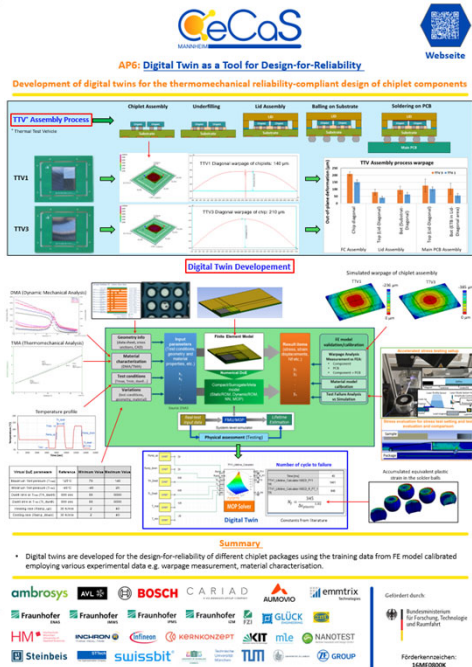
### Device Analysis:

Structural Integrity / Geometry / Warpage as  $f(t/T)$  / Functionality

... is used to build a Digital Twin for reliability

-> a versatile tool to calculate product remaining lifetime  
depending on load cycles

Ghanshyam Ghadya, Sven Rzepka, FhG ENAS & Volker Bader, Karl-F. Becker, FhG IZM

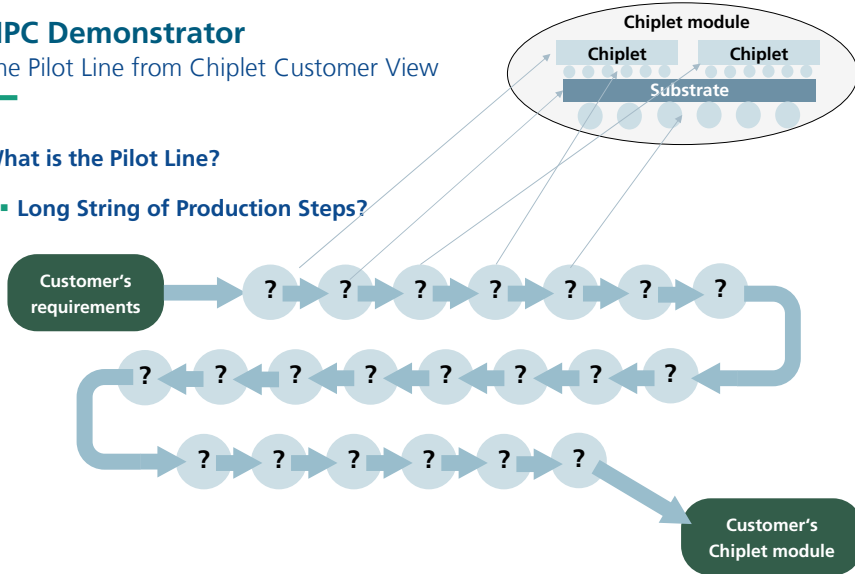


# HPC Demonstrator

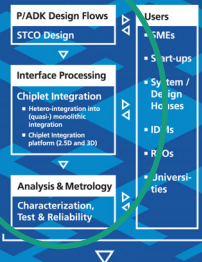
The Pilot Line from Chiplet Customer View

## What is the Pilot Line?

- Long String of Production Steps?



Advanced Packaging and  
Heterogeneous Integration  
for Electronic  
Components and Systems



Application Solution developed  
under the EU Green Deal

Partners:





# HPC Demonstrator

## The Pilot Line from Chiplet Customer View

### What is the Pilot Line?

- Based on customer requirements, specific Chiplets are designed & manufactured, general IP block Chiplets and passives are sourced, a system is designed based on advanced packaging technology selection, interposer/substrate are procured, the system is assembled and tested ...
- Sounds straight forward, but ...
- ... it's rather a complicated mesh!

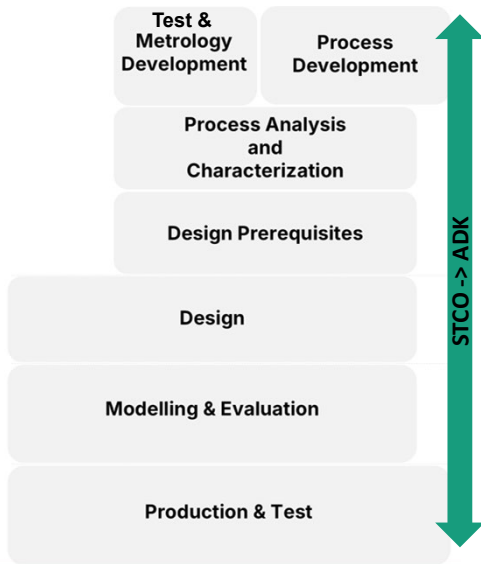


# HPC Demonstrator

The Pilot Line from Chiplet Customer View

## Research Areas within APECS are

- **Process Development & Metrology Development**  
(incl. Test Methodology & Strategy Development)
- **Process Analysis & Characterization**  
(STCO towards process modeling and ADK)
- **Design Prerequisites**  
(IPs, KnowHow, PDK/ADK)
- **Design (-> System Design )**
- **Modelling & Evaluation**  
(of the designed system -> Digital Twin)
- **Production & Test**  
(aligned with customer needs/data model)



# Industrie 4.0

## Digitalization at IZM – in a research environment

At Fraunhofer IZM, we are working on digitalization ...

... through digitalised production planning using a wide variety of tools -> **MES/PMS**

... through the development of data sets and material laws for evaluating property changes, e.g. due to thermal ageing (Mature with IFAM) or moisture storage, e.g. to optimise service life predictions -> **Digital twin of materials in the area of design/reliability**

... through the abstract description of processes (flow chart, Ishikawa diagram) and the recording of a wide variety of production data and the normalised summarisation of the data in order to optimise knowledge-based/AI-supported processes. -> **Digital twin of production processes**

... by analysing process flows and variants to evaluate manufacturing costs and ecological implications  
-> **Digital twin for cost/eco-balancing**

... AI-supported by correlating product quality and ZV analyses -> **Digital twin for product reliability**

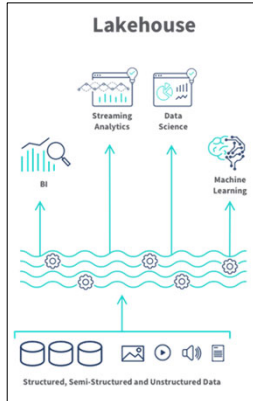
... by deriving design parameters through technology analysis using statistical methods -> **ADK/PDK**

➤ **Digitalization and AI are an integral part of our research work!**



# Packaging Technology in the Digital Realm

## Digital Twins & AI-related Tools



Automated data acquisition and processing is the foundation of all data-based technology optimization - ADAPT

Ontologies are a key enabler for system technology co optimization [STCO] in holistic data landscapes

Increasing performance needs and cost reduction requirements call for data-based process optimization in the design phase of a product

Advanced data analysis needs AI related tools to manage data of and optimize complex process chains

As the essence of digitization, Assembly Design Kits (ADKs) make technology available to system designers



Fraunhofer Institute for Reliability  
and Microintegration IZM

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