Power Electronics – Stragtegies for Cost Effective Production

Fraunhofer IZM

Fraunhofer Institute for Reliability and Microintegration IZM

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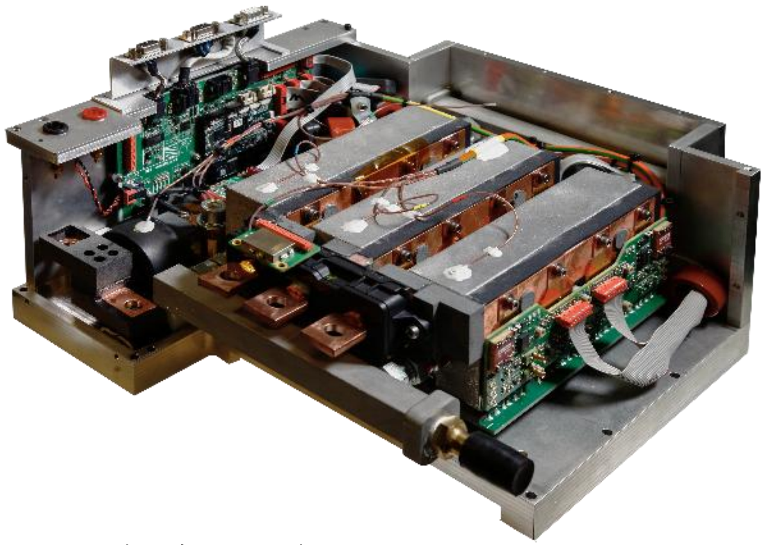
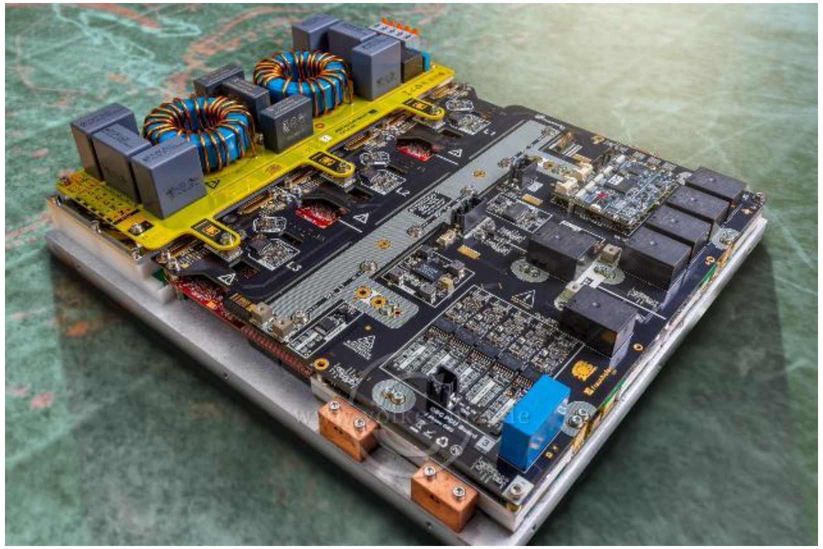
Where is Power Electronics developing to?

- The need for power electronics is rising tenfold due to electrification of our society
- Resource efficiency has to rise
- Electrical efficiency is mandatory
- High production values and automation
- Recycling to be considered



250kW/l motor drive

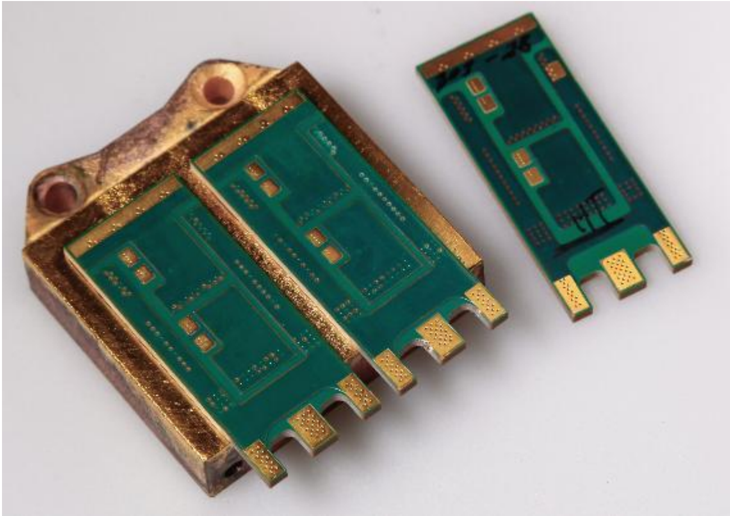
Solutions:
- Faster switching , smaller passives
- Circuit development adapted to production methods
- Deep engineering with algirithm aided optimization



7kW/l OBC with flat magnetics

Scaling produktion processes and low switching losses

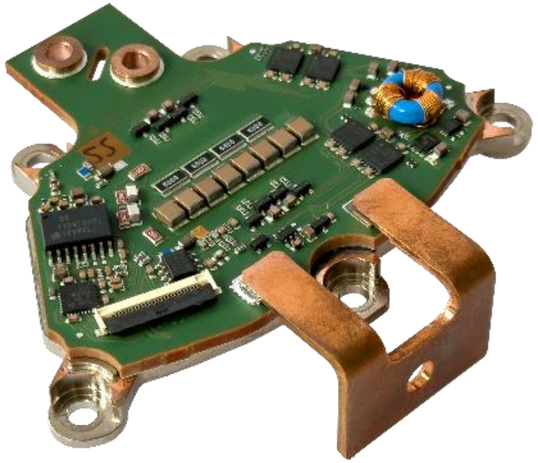
How to get there?

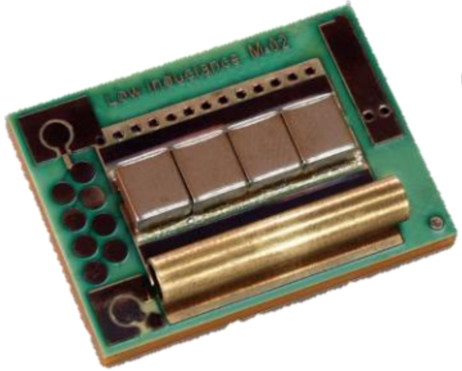


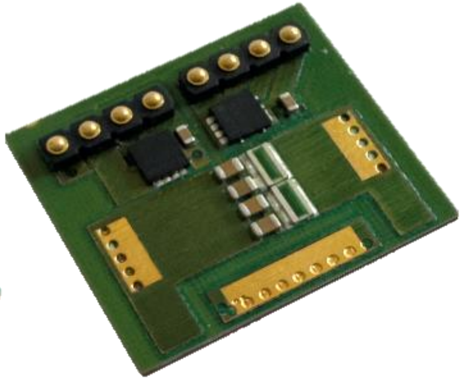
Use of manufacturing methods with high lot sizes:

PCB embedding on ceramics

- PCB lot size is 60 x 60 cm
- Power module with 600Arms 1200V can be built in a size of 24cm² in Embedded auf Ceramics technology
- PCB embedding offers design freedom for electromagnetic optimizartion





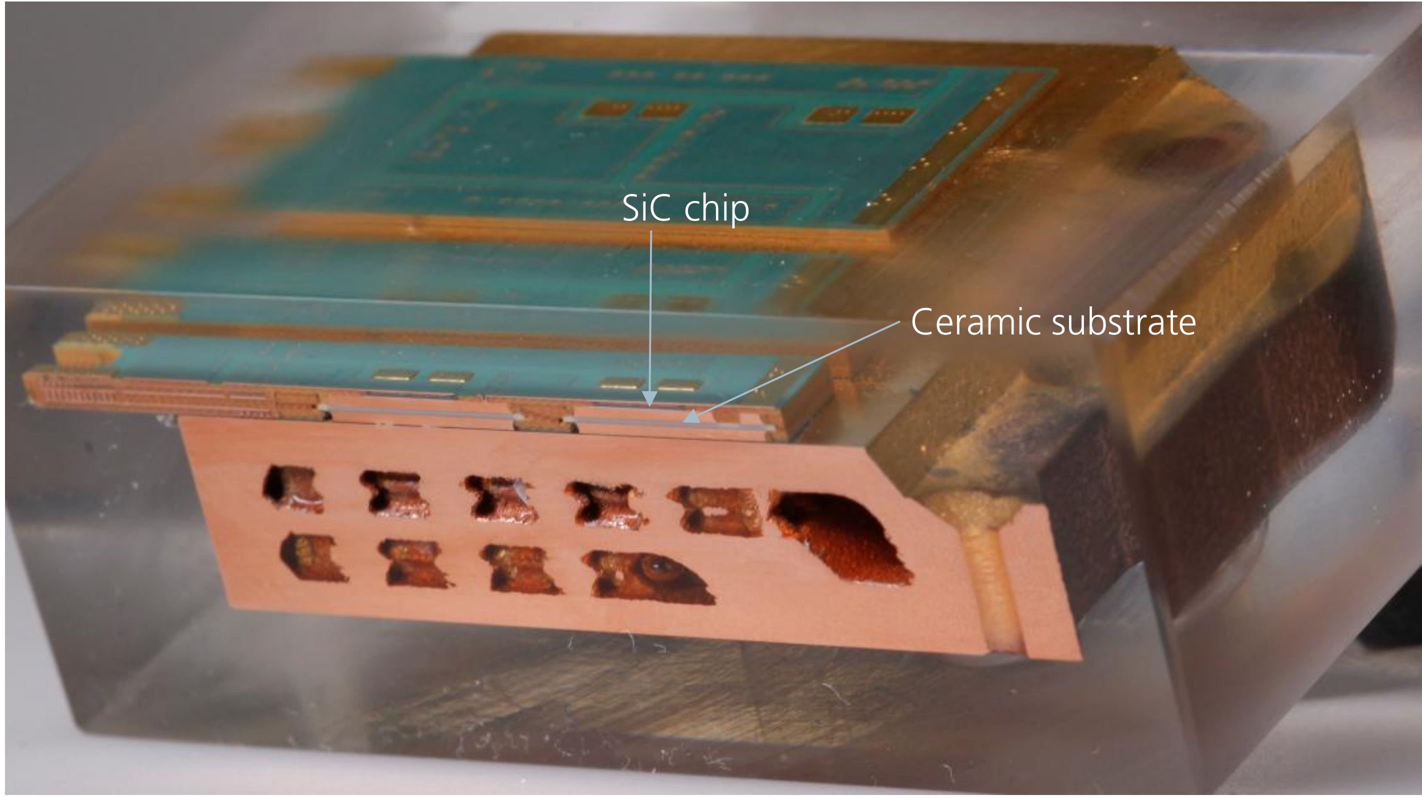


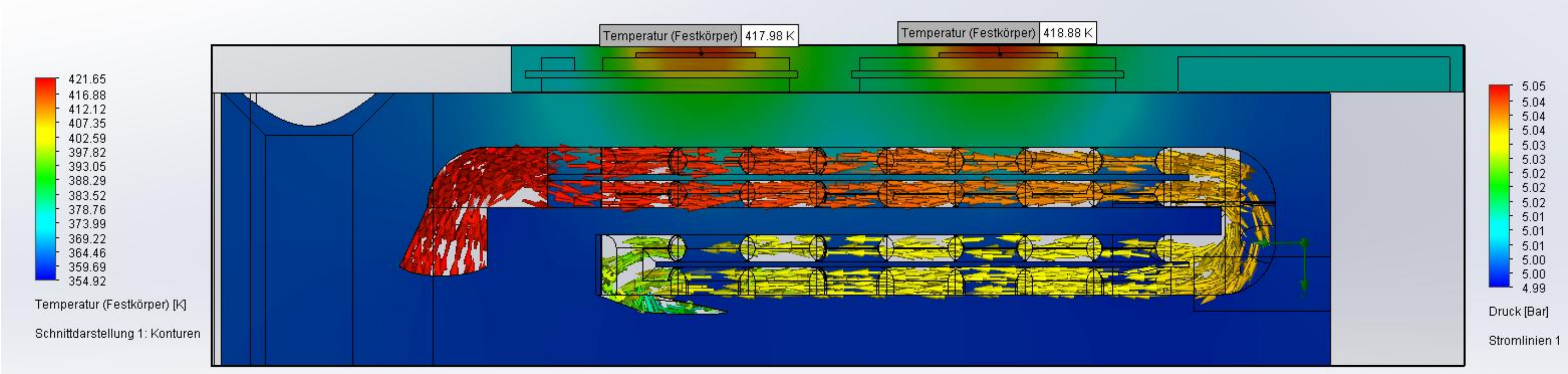
High Power density

How to achieve? The thermal path

Combination of ceramic substrate and PCB

- SiN substrat in the PCB for best thermal performance
- In this example sintered to a 3D printed copper cooler
- $R_{thj\text{-}fl}$: 0.46K/W per 5x5mm² chip
- Power density is a key for low production cost



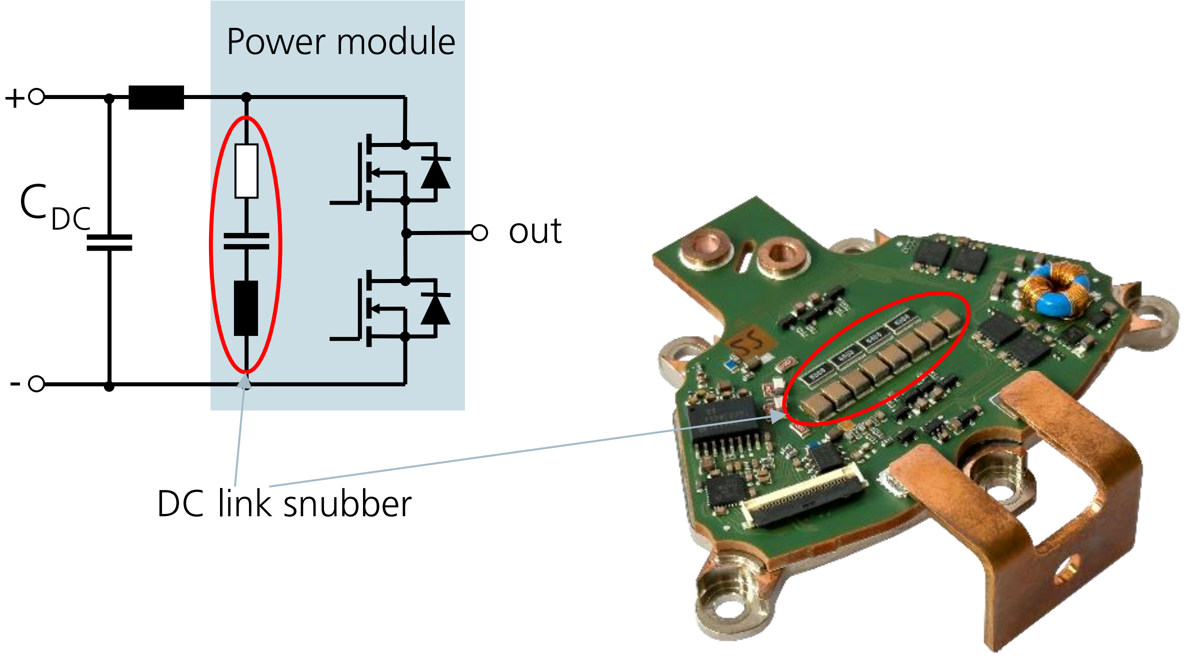


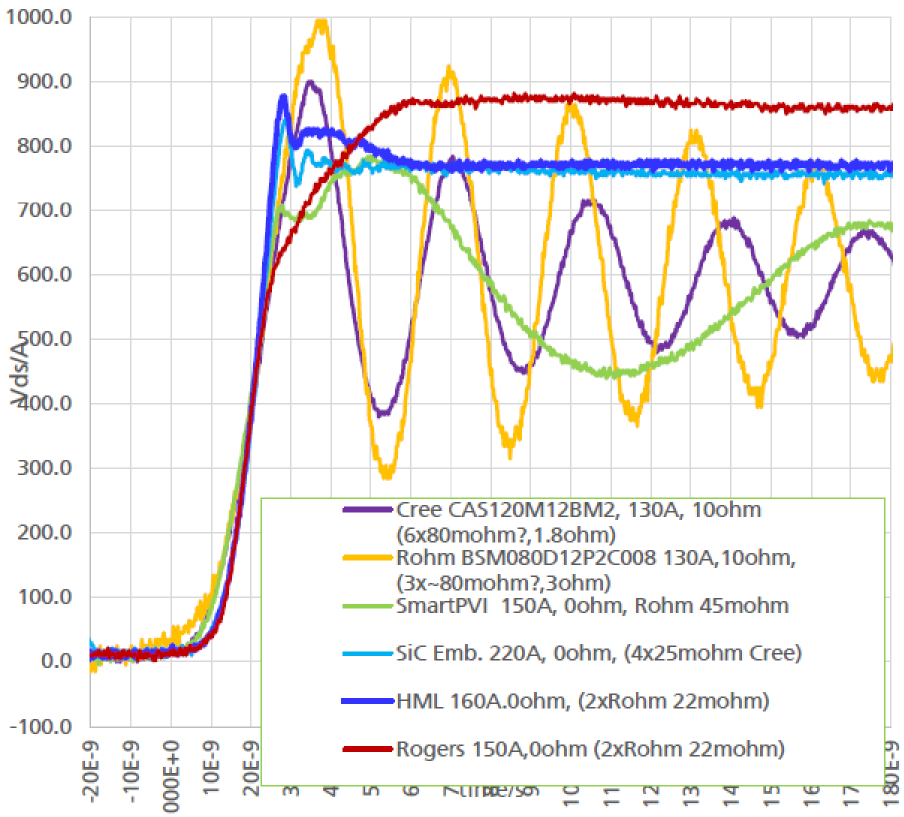
Lower switching losses: more power with less semiconductors

Module wih DC link snubber: total switching cell inductance 1.5nH

Embedding technology enables DC link snubber on the module

- 0Ω Gate resistance possible, fastest switching without ringing
- Switching losses reduced by more than 70%





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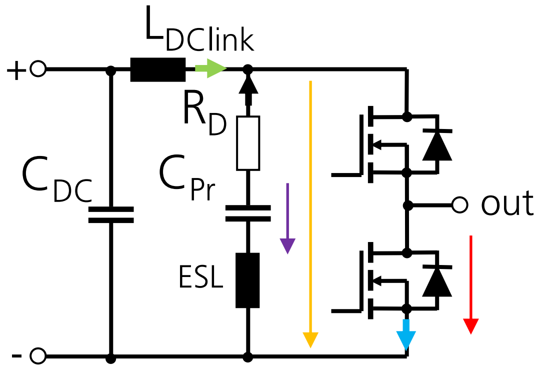
Lower switching losses: more power with less semiconductors

Module wih DC link snubber: total switching cell inductance 1.5nH

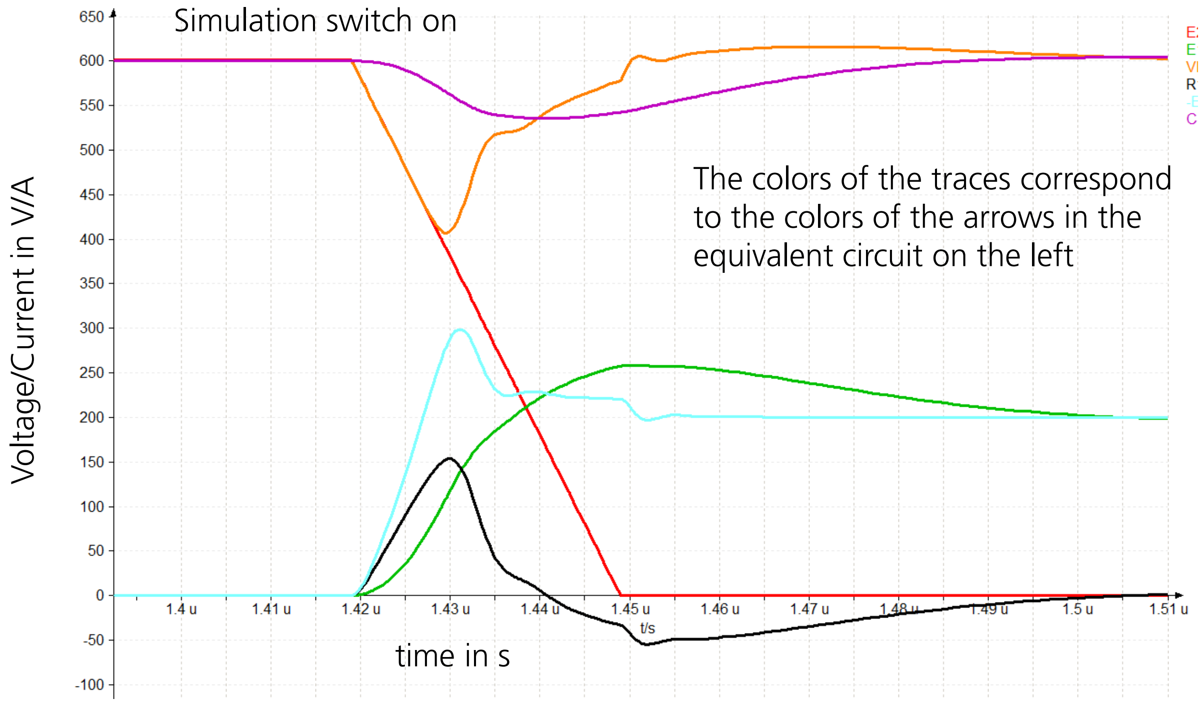
Bin case of 70% conduction losses and 30% at peak power the total losses of the Mosfets can be reduced by 20%

- 10% more power with the same semiconductors or
- 10% less semiconductors or
- 20% lower Tj -> longer lifetime

Funktion of a DC link snubber in an embedding power module



R_D: 0.9 Ohm
C_{Pr}: 26nF
LDClink: 10nH
Switching Mosfet (LS) modelled by voltage source only
Blocking Mosfet (HS) by Coss only

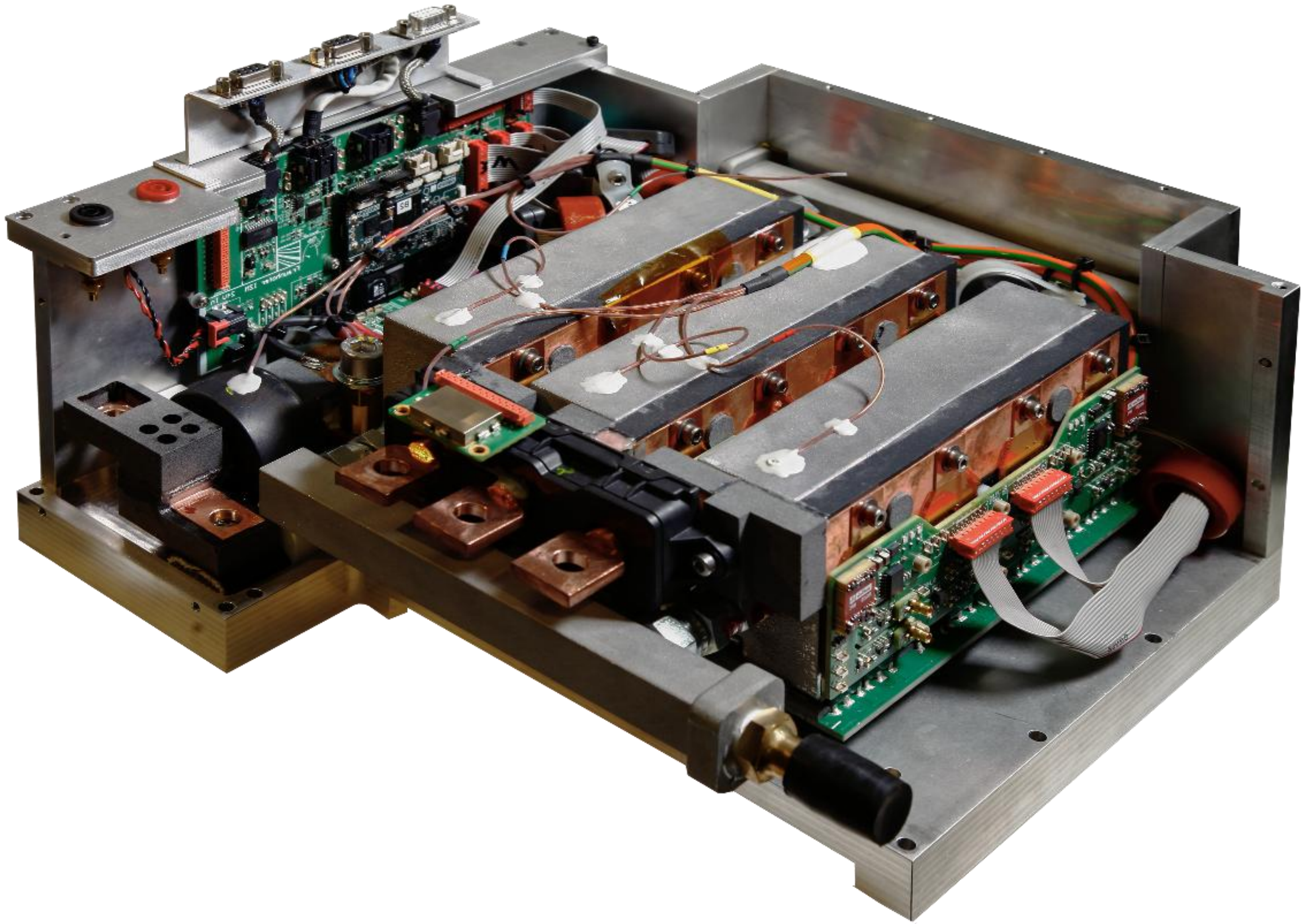


Motor inverter with 750 kW at 3l volume

How to get there?

Deep engineering;

- Power modules in embedding on ceramics technology
- 3D printed copper cooler, cooled polyacrylate capacitor
- DC link as PCB (at 750kW!)

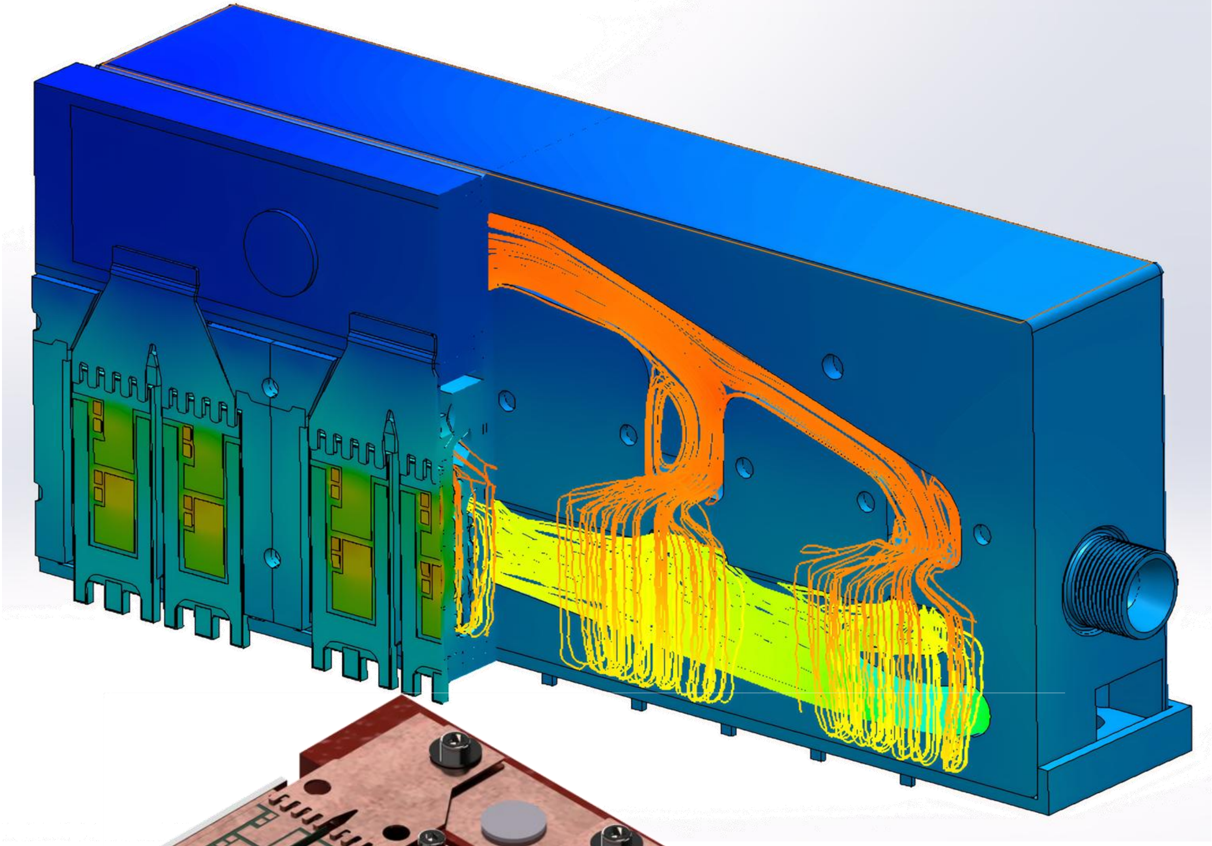


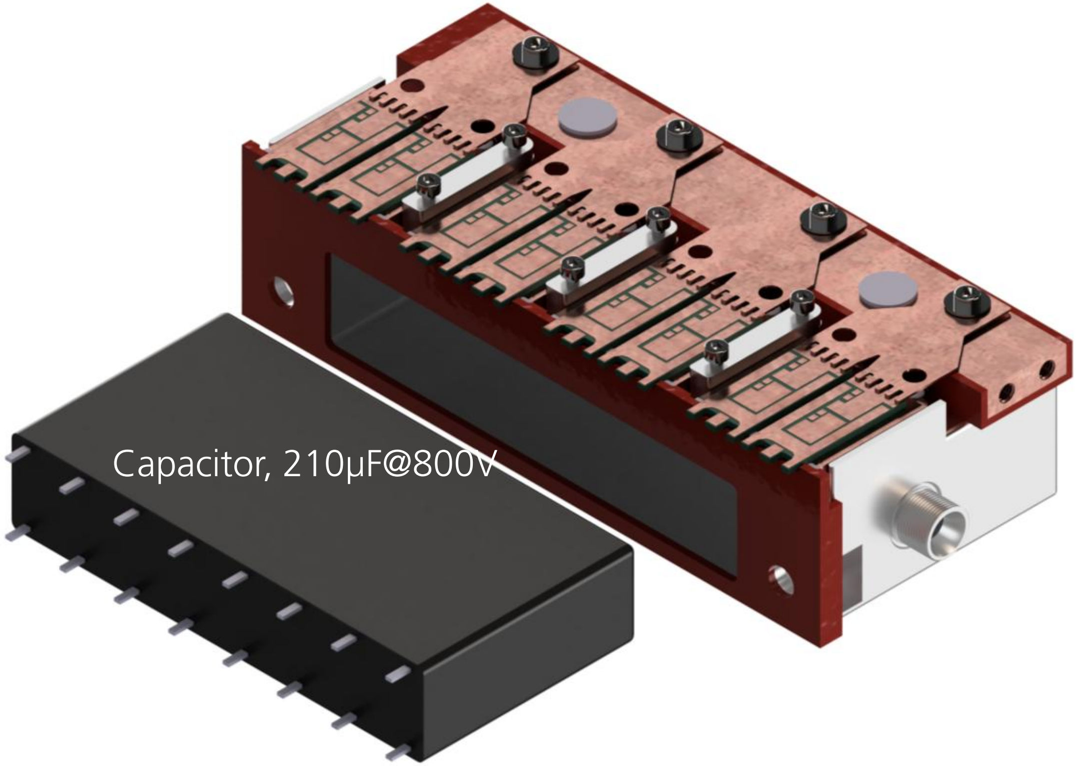
High Power Density inverter

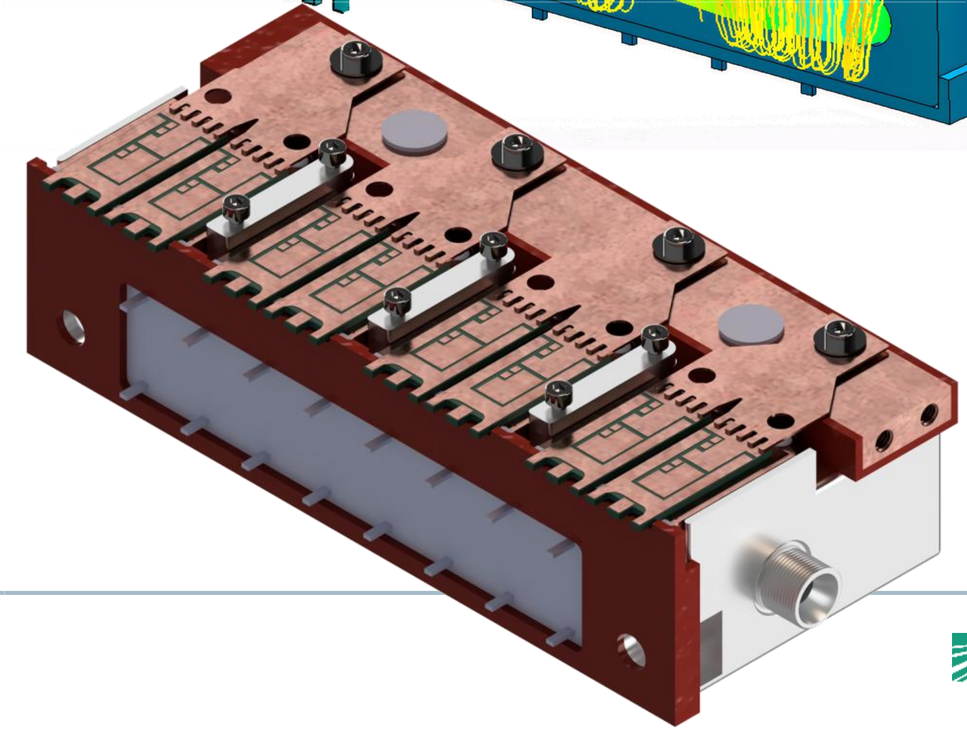
How to achieve it? Cooling the capacitor

3D printed aluminum water duct

- 4 heat sinks with together 8 modules per switch (8 SiC semiconductors parallel per switch)
- Polyacrylate capacitor built in the water duct for good cooling







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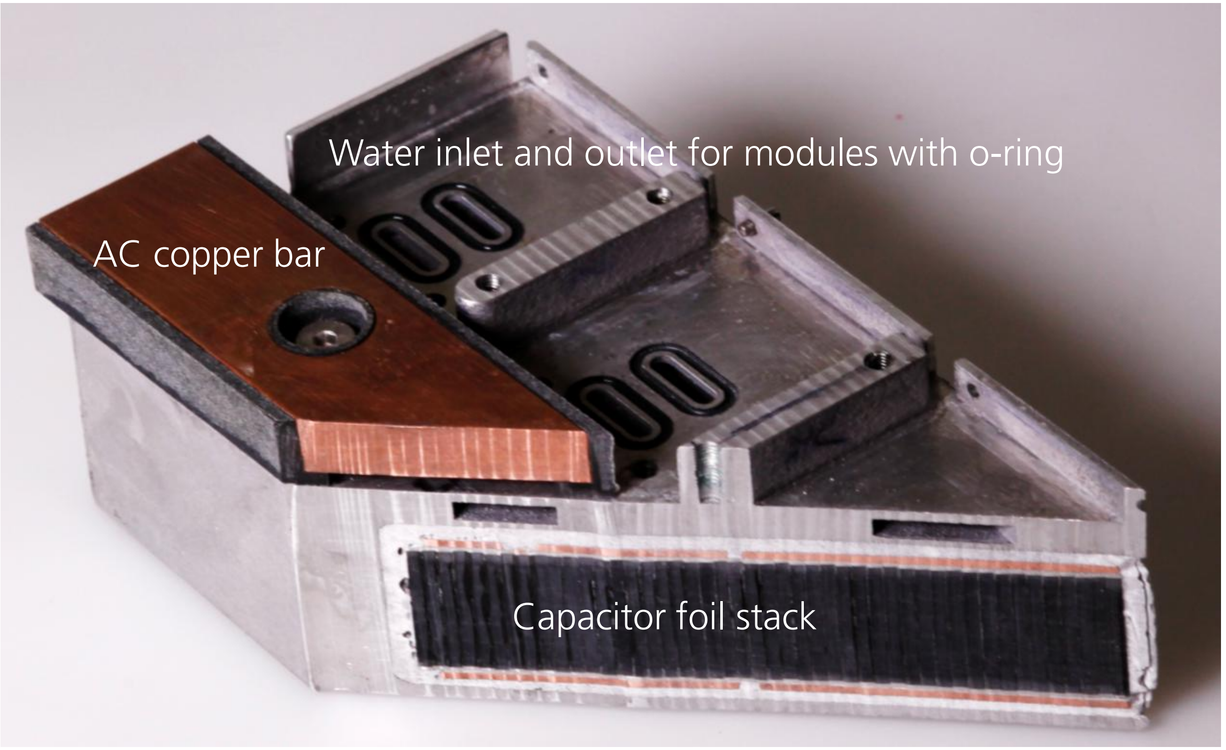
High Power Density inverter

How to achieve it? Cooling the capacitor

Capacitor integrated in the water duct

- Good cooling of the capacitor to increase current ripple capability
- Encapsulation of the polyacrylate capacitor to ensure humidity resistance
- Copper contacts with pins to enable soldering into PCB style DC link
- Cooled AC copper bar

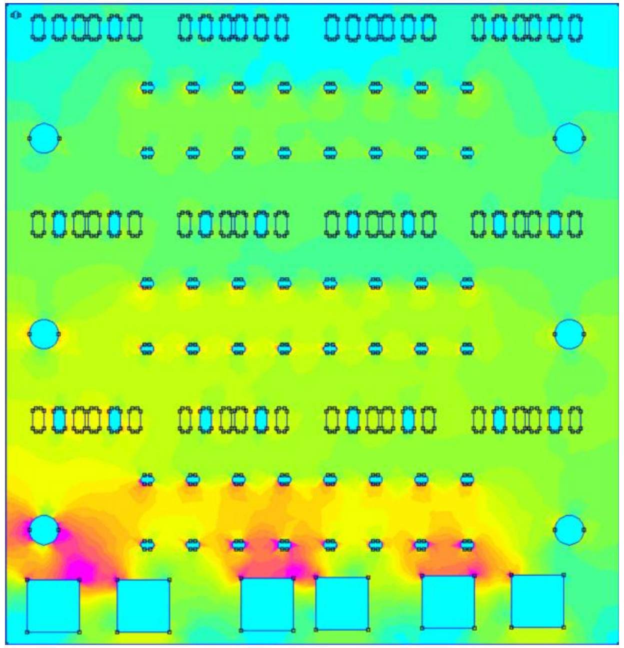


High Power Density inverter

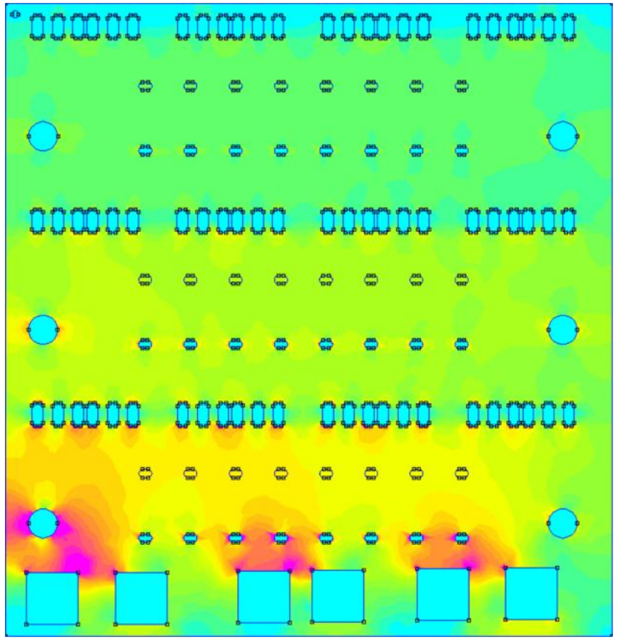
How to achieve it? The DC link bus

Calculation of losses in the DC link for a PCB with 8 layers 100µm copper

- DC terminals to capacitor and modules, capacitor to modules, free wheeling

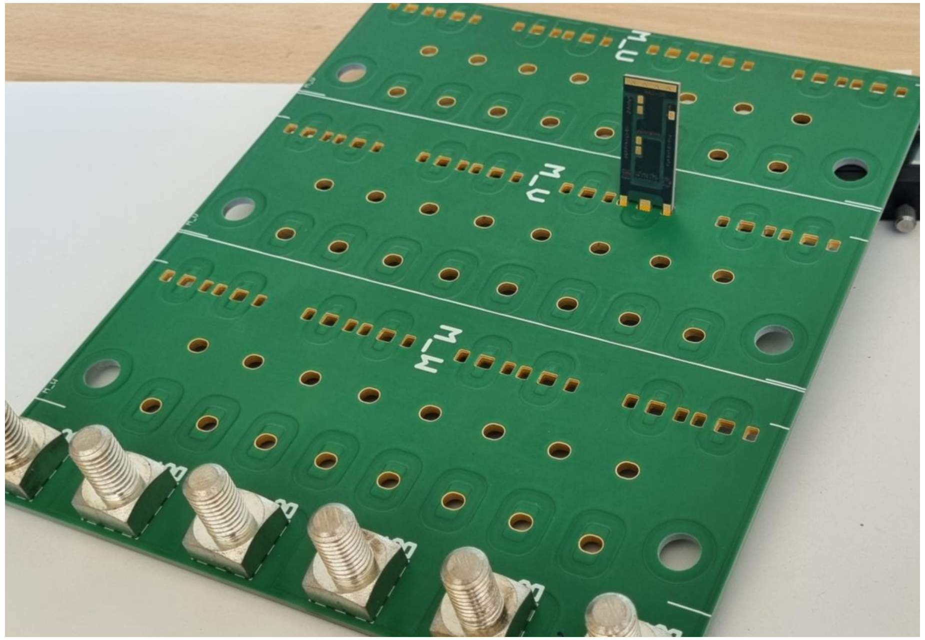


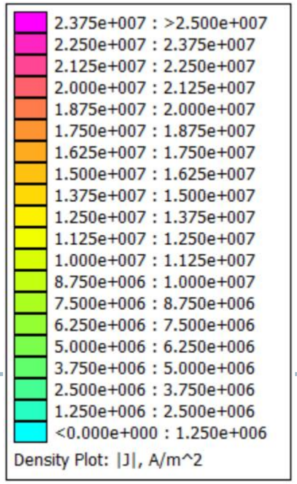
- PowerLosses DC+ to CAP+ 18.53 W
- Weighted_PowerLosses DC+ to CAP+ 3.15 W



- PowerLosses is DC+ to Phases+ 21.03 W
- Weighted_PowerLosses is 17.45 W

- DC link PCB with one module





High Power Density inverter

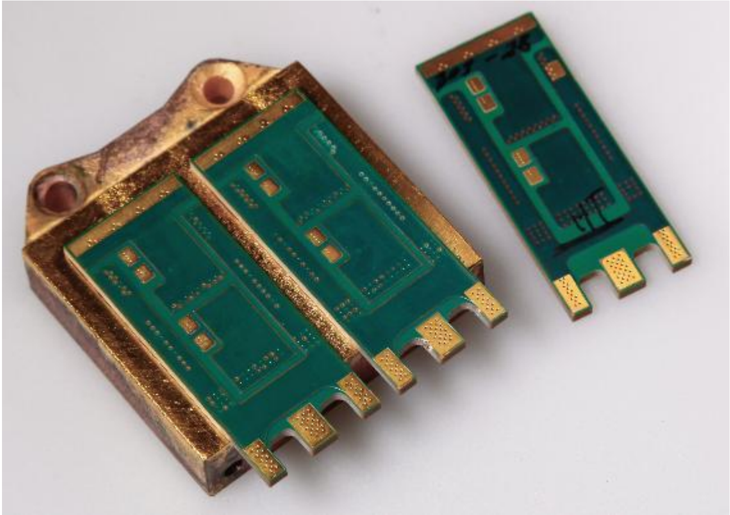
The DC link bus

Half bridge modules connected in parallel (eight semiconductors)

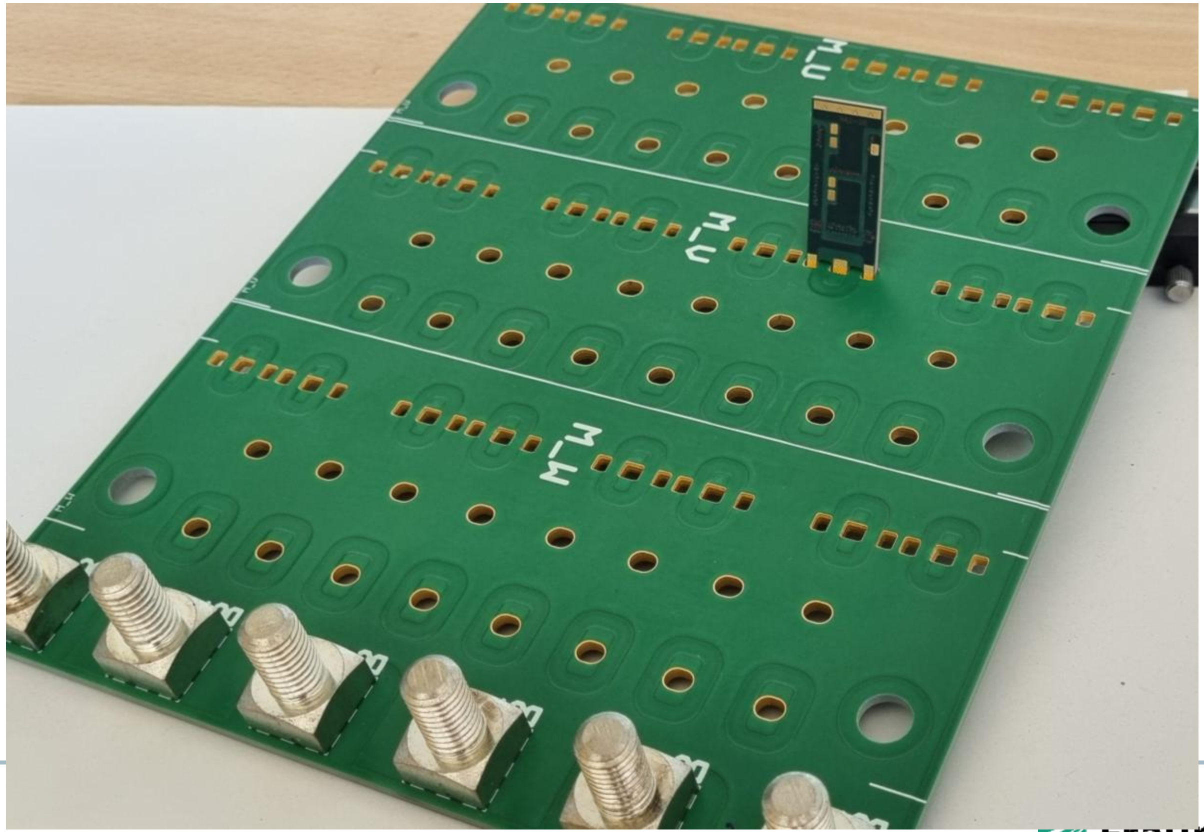
- New way of paralleling chips: interconnect by soldering, scalable
- No issues with ringing, it worked immediately

-> 800A switching at max speed

Half bridge module with single chips (right),
2 modules sintered onto a heat sink



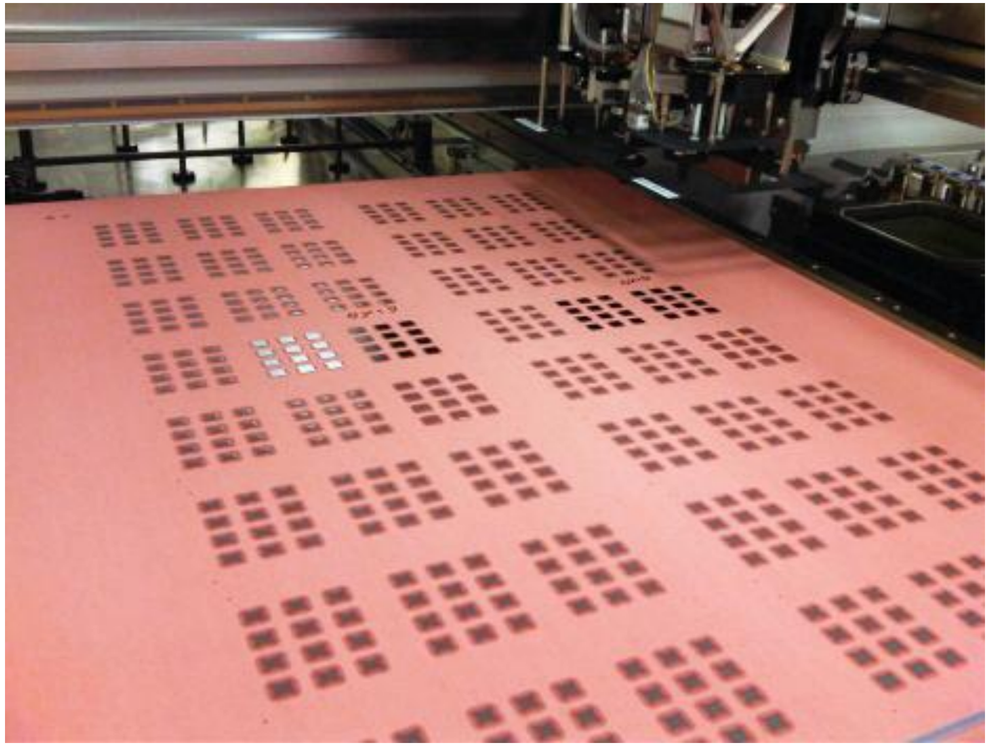
DC link PCB with one module



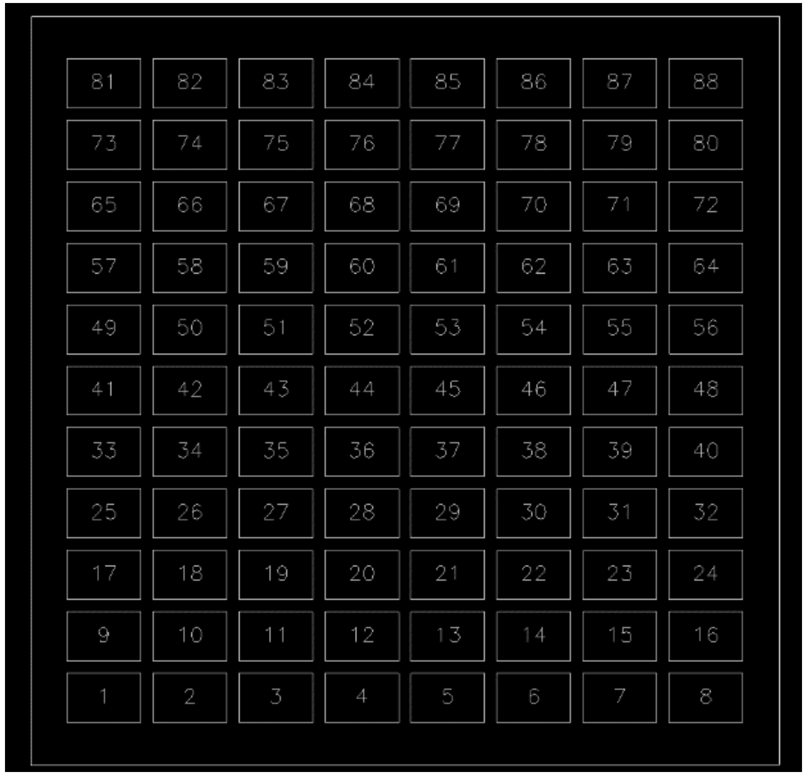
Scaling production processes

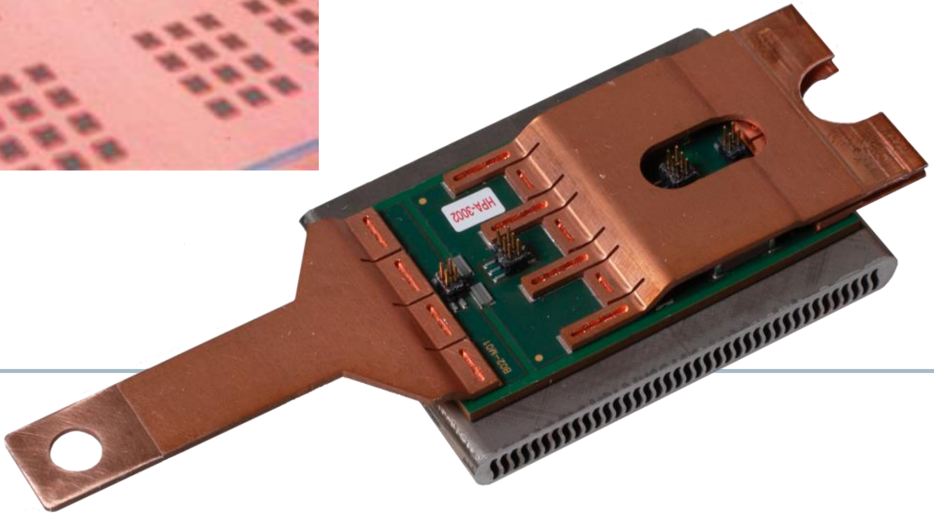
How to get there?

PCB lot with 60 x 60 cm²



88 moduls with 600A/1200V can be produced on one lot
-> Demonstration at next PCIM





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Produktionsprozesse skalieren: reduziert Produktionskosten

How to achieve it? Power module technology

Embedding on ceramics technology

- PCB base plate is created with SiN substrates inlays
- SiC semiconductors are silver sintered to AMB
- PCB prepreg material with and w/o cutouts for semiconductors and thin copper foil is laminated on top
- Laser drilling for top side interconnect vias. Then galvanic copper build up and structuring is carried out
- Normally a second PCB layer is built up on top

Layup of PCB core material and AMB inlay

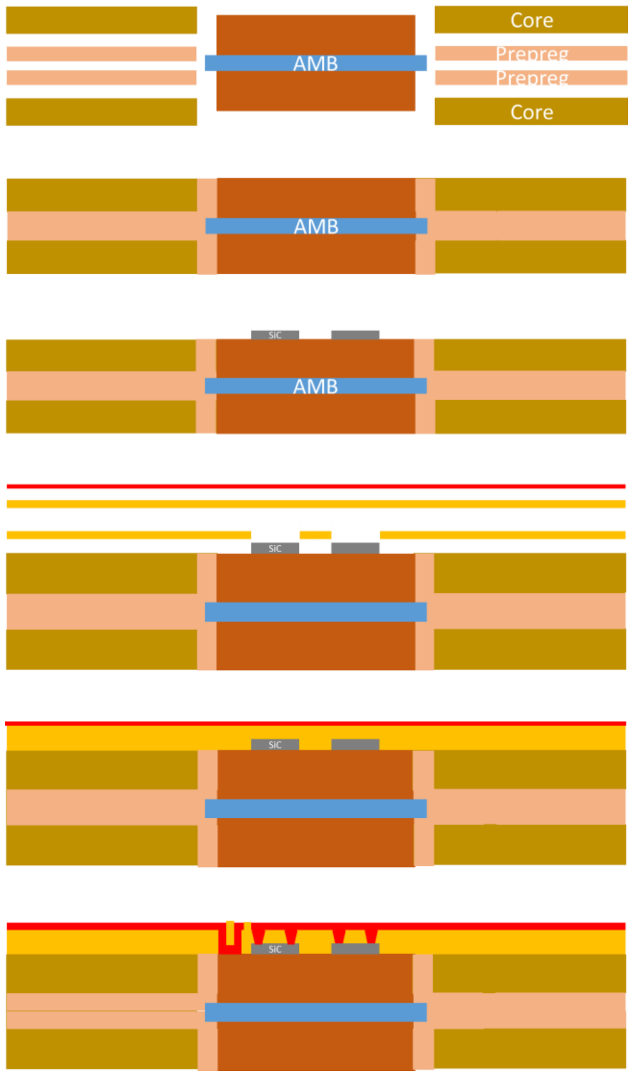
Embedding by vacuum lamination

Assembly of SiC by Ag sintering on large substrate

Layup of prepreg

Embedding of SiC by vacuum lamination

Laser via formation to SiC, metallization and routing



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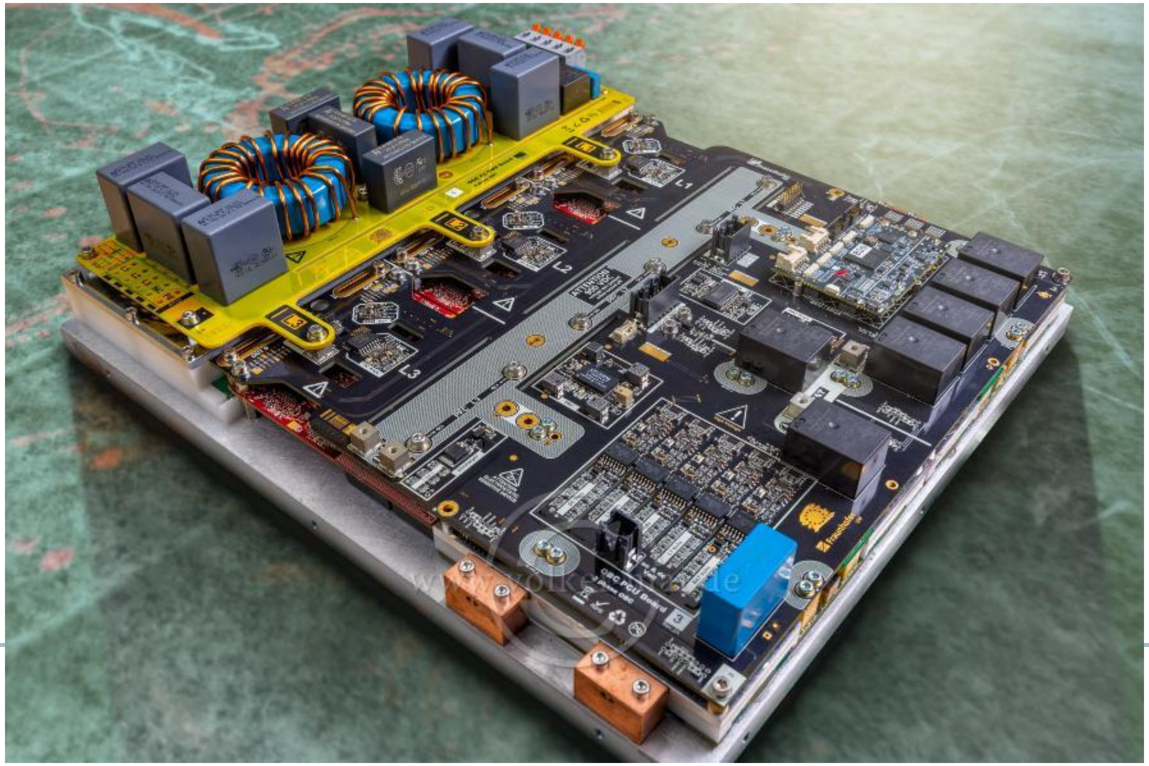
Automated production

How to reduce production cost?

- Automated production: SMD assembeled semiconductors (top side cooled) and magnetics with PCB windings
- Circuit development has to be adapted to design parameters of PCB windings



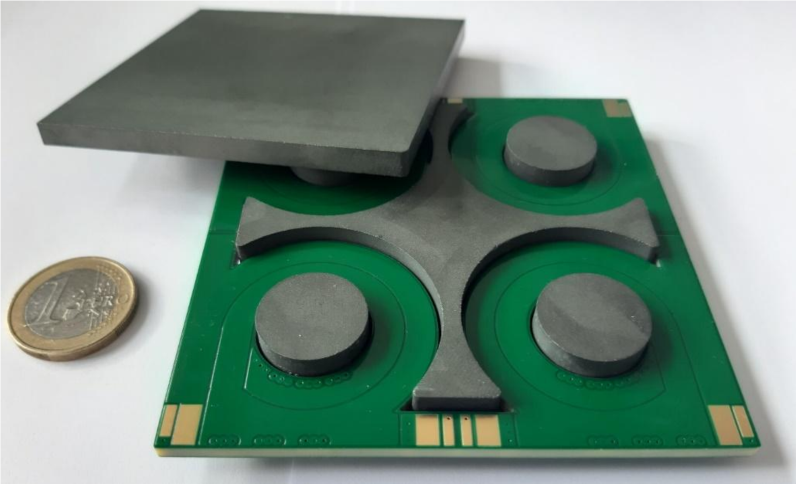
7kW/l OBC flat magnetics (22kW)

PCB style magnetics

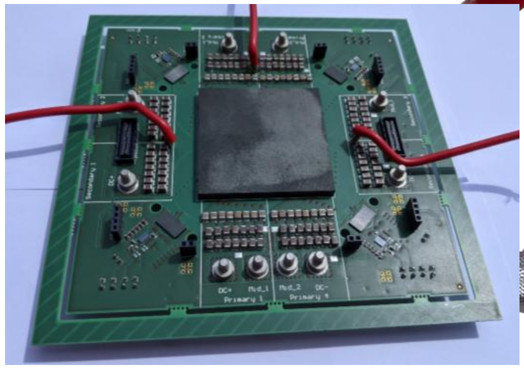
Where is the upper limit in power?

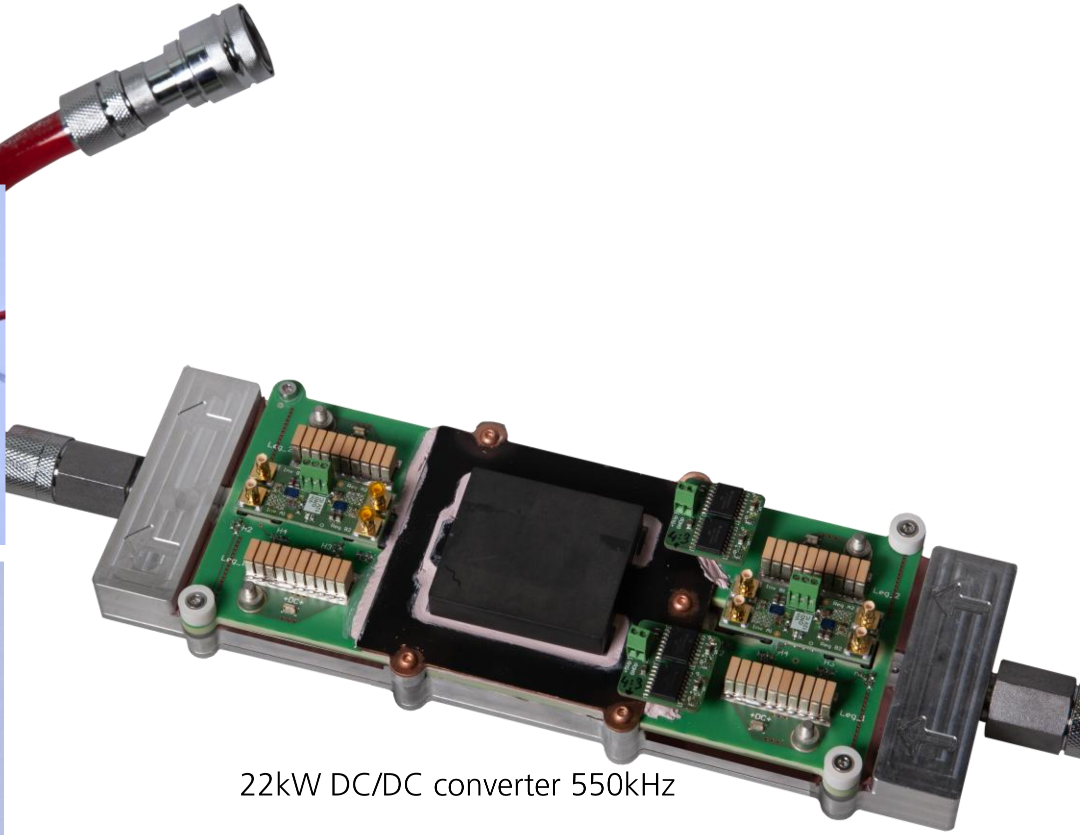
- Eddy current effects are significant in higher diameter ferrites
- Thermal contact with gap filler is mandatory for PCBs

Coupled PFC inductor (3 for 22kW, 140kHz)



11kW DC/DC converter 1MHz



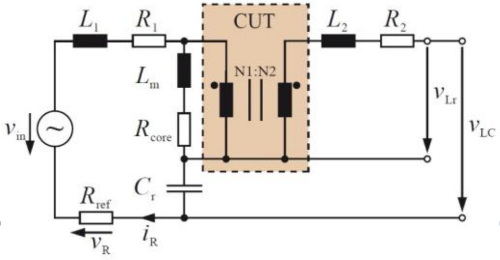


22kW DC/DC converter 550kHz

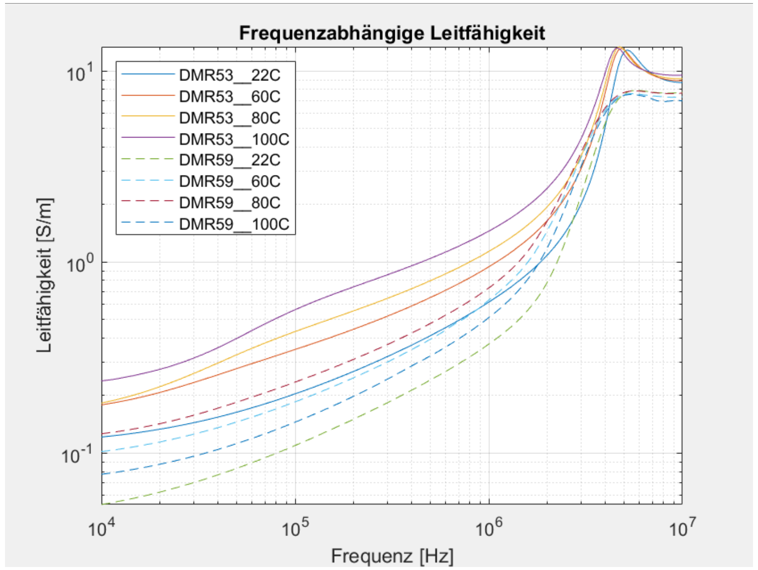
PCB style magnetics

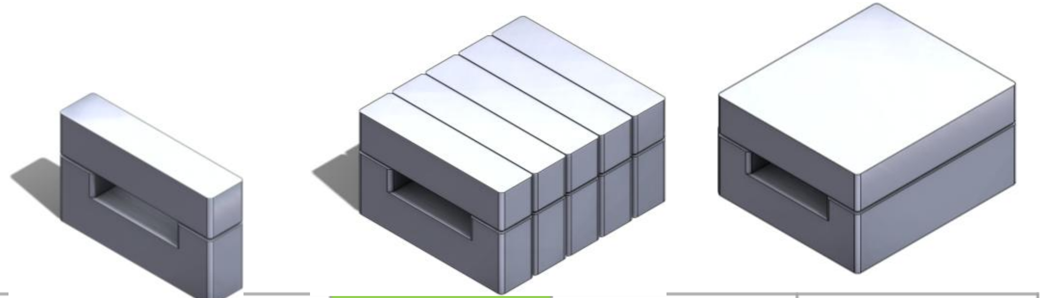
Where is the upper limit in power?

- Big ferrite cores show more losses
- Pressure increases losses
- Ferrite surfaces increases losses



Frequency dependend conductivity





	Einzelstück 10mm	geblecht 5mm	geblecht 10mm		vollmaterial	
Temp. 80°C	100mm², 10cm³	10*100²,50cm³	5*100mm², 50cm³		500mm², 50cm³	
Luftspalt	ohne	mit	ohne	mit	ohne	mit
1MHz, 40mT	2,2W	-	23W	12W	40W	40W
1MHz, 50mT	5,5W	5W	41W	23W	70W	65W

22kW DC

50kHz

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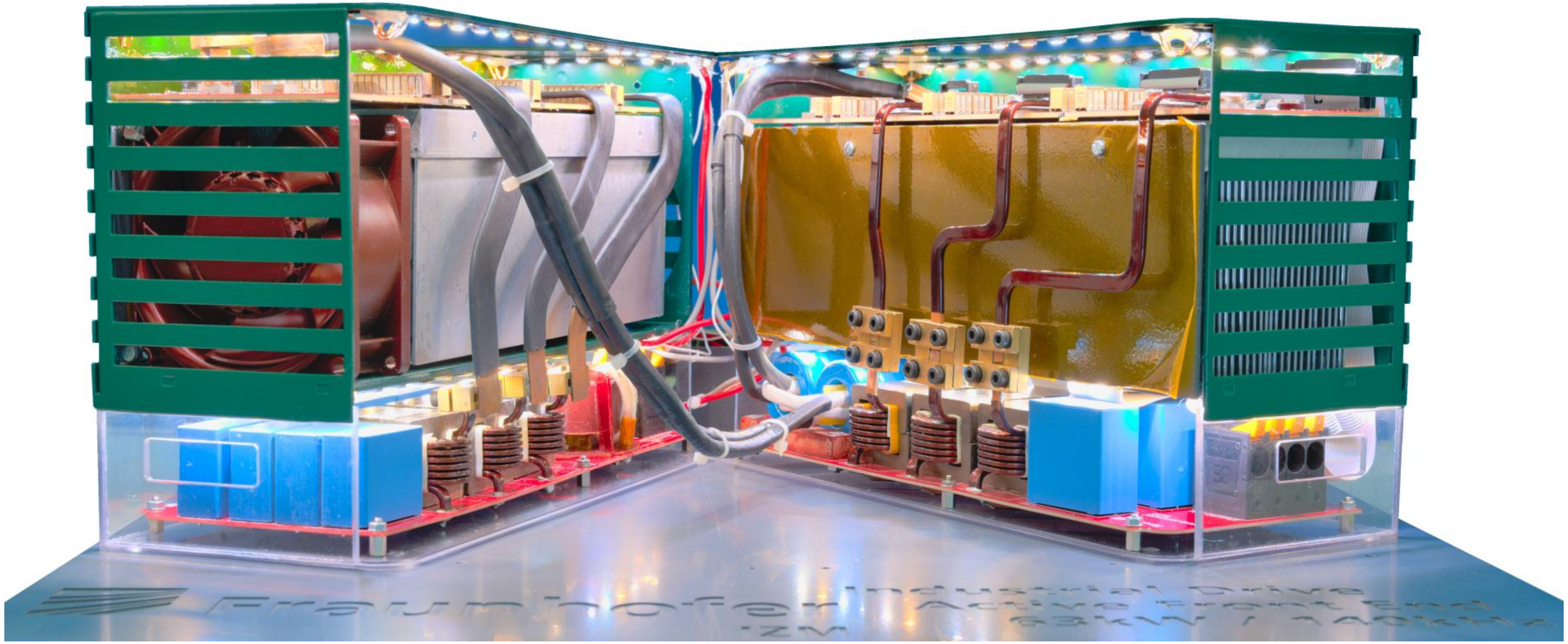
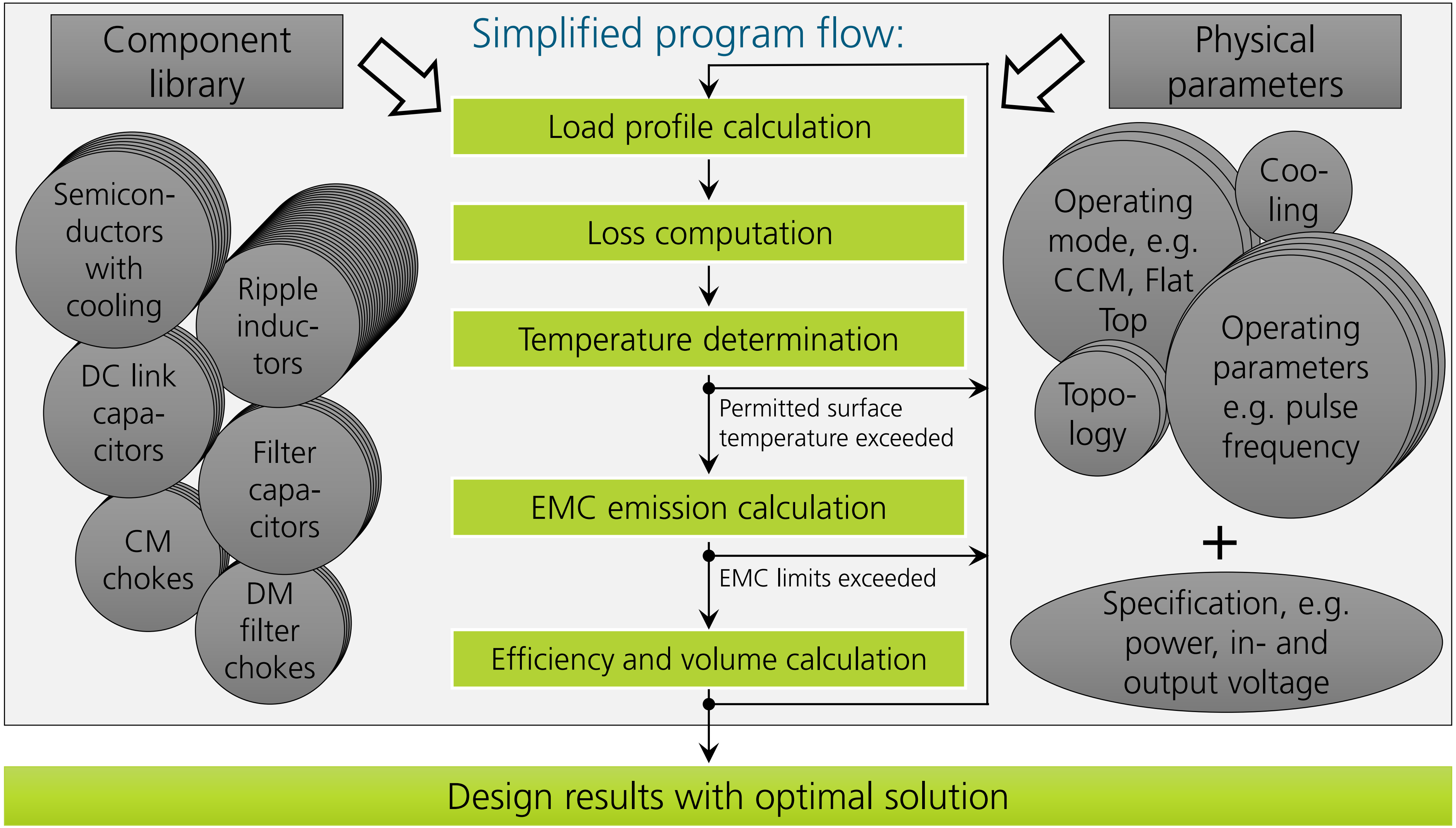
How to optimize power electronics?

Pareto front optimization of a bidirectional motor drive 63kW

- Fully filtered grid and motor side
- Pareto-front optimization of switching frequency, semiconductors, inductor and filters



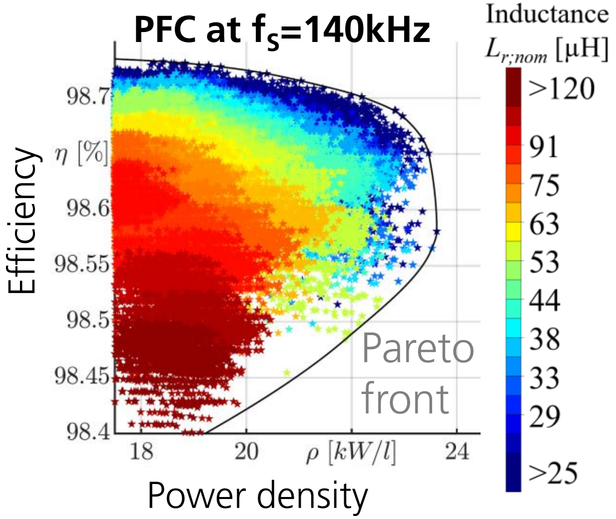
Optimizing algorithm for inductor, switching frequency, control and EMI

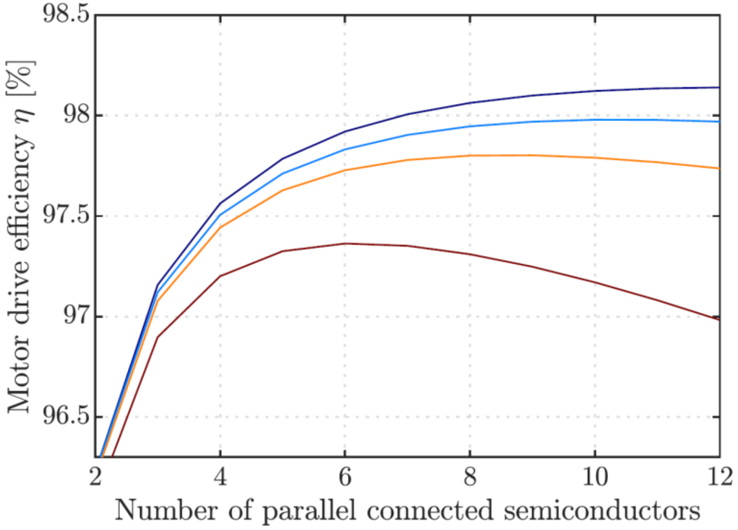


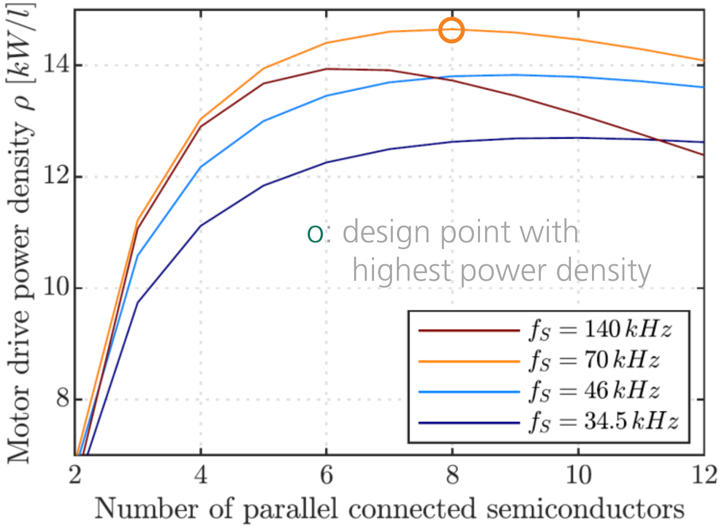
- Component library: required data of each component to calculate operating behavior, losses, volume, EMC emissions etc.
- A large number of design combinations can be calculated in a short time
- This allows the optimal solution to be extracted

Optimizing algorithm for public (50Hz) grid connected inverters

- Computing time for thousands of combinations is in the minute range
- Optimum configuration can be determined from the optimization for several switching frequencies
- Further investigation options:
  - optimal number of parallel connected semiconductors,
  - EMC filter optimization,
  - loss distribution in the semiconductors and ripple inductors in dependence on the mains angle,
  - determination of the loss optimal dead time in dependence on the load
- **Design result of a 3-phase motor drive (P=63kW, f_G=50Hz, V_G=230/400V, V_{DC}=610V)**







Conclusion

Technical progress goes on in power electronics

What are the drivers?

- Deep engineering as basis for squeezing out optimization potential in a mature technology
- Adapting to manufacturing technologies for cost reduction
- Electromagnetic design as enabler for fast switching at high power
- Optimization supported by self developed algorithms. Artificial intelligence does not yet play a significant role, as in most cases not enough training data is available

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