

Electronic Packaging Days 2025

Ivan Ndip

RF Packaging Architectures and Design for Communication, Sensing, Computing and AI Applications

Outline

- ❑ Bandwidth: Driver of Innovation in Radar Sensing, Communication, Computing & AI Applications
- ❑ Bandwidth-related Design Challenges at Higher Frequencies for Communication & Sensing
- ❑ IZM's Unique & Holistic RF Design Approach: From Materials to Modules
- ❑ Chiplet Modules for High Performance Computing (HPC) & AI Systems
- ❑ IZM's Methodology for Signal & Power Integrity Design of Chiplet Modules
- ❑ Key Take Aways

Bandwidth: Driver of Innovation in Sensing, Communication, Computing & AI

Radar Sensing

$$\Delta R = \frac{c}{2 BW}$$

- More BW => Higher range resolution
- Example: Automotive radar: 24 GHz (0.5 GHz) => 77/79 GHz (4 GHz) => D-Band (14.5 GHz); Industrial liquid level radar (D-band)
- Move to higher frequencies for more BW

Communication

$$C = BW \cdot \log_2(1 + SNR)$$

- More BW => Larger channel capacity, higher data rates, more device connectivity/unit area
- Example: 1G to 4G (< 3GHz); 5G (up to 40 GHz); 6G (up to 175 GHz); Data center communication
- Move to higher frequencies for more BW

Bandwidth (BW)

High-Performance Computing (HPC) & AI

$$P = \min(P_{peak}, BW_{peak} * I)$$

- More BW => Higher performance of HPC & AI systems
- Increase parallel connections between processor & memory for more BW

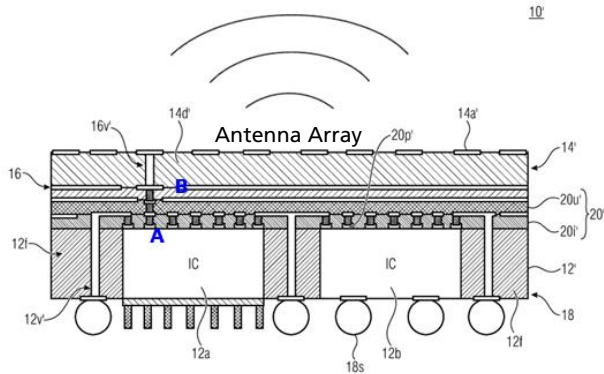
IZM's Unique & Holistic RF Design Approach: From Materials to Modules

Application-Specific RF Packaging Architectures

Application-specific RF packaging architectures which inherently ensure lower losses, higher antenna gain, scalability & EMC



Thermo-mechanical reliability, manufacturing, Green & cost requirements...



Fraunhofer IZM (Germany) - Fan-out WLP AiP
(US-Patent: US10978778B2; EU-Patent: EP3 346 493B1)

$$EIRP = P_{PA} + G_{ant.} - L_{AB}$$

$$SNR = \frac{P_{PA} G^2 \lambda^2 \sigma}{(4\pi)^3 R^4 k T_s B_n L}$$

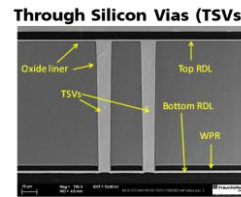
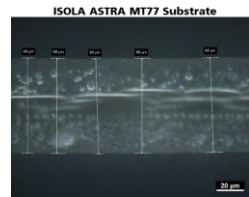
RF Characterization of Packaging Technologies

Measurement-based extraction of Dk and Df of packaging materials (processed & non-processed) in dependency on frequency, temperature & aging

RF characterization of packaging structures up to 500 GHz



Fabrication and aging of test samples

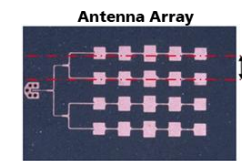
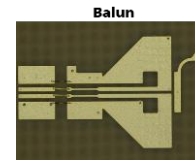


Development of Application-Specific Package Integrated RF Components using M3-Approach

RF design & test of package integrated RF components (e.g. antennas, filters) based on characterized packaging technologies



Fabrication and aging of test samples

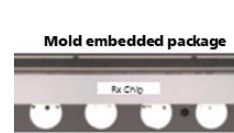
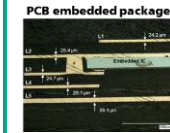


Development of Application-Specific RF Packages using M3-Approach

RF design, layout & test of application-specific packages with integrated RF components



Thermo-mechanical design and fabrication of package samples

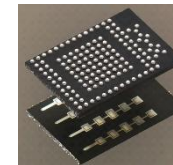


Development of Application-Specific RF Front-end Modules

Layout & test of segments of functional RF front-end modules



Assembly of transceiver chips, passive components & fabrication of RF front-end modules; Assembly onto system-board



6G THz module



60 GHz medical radar module



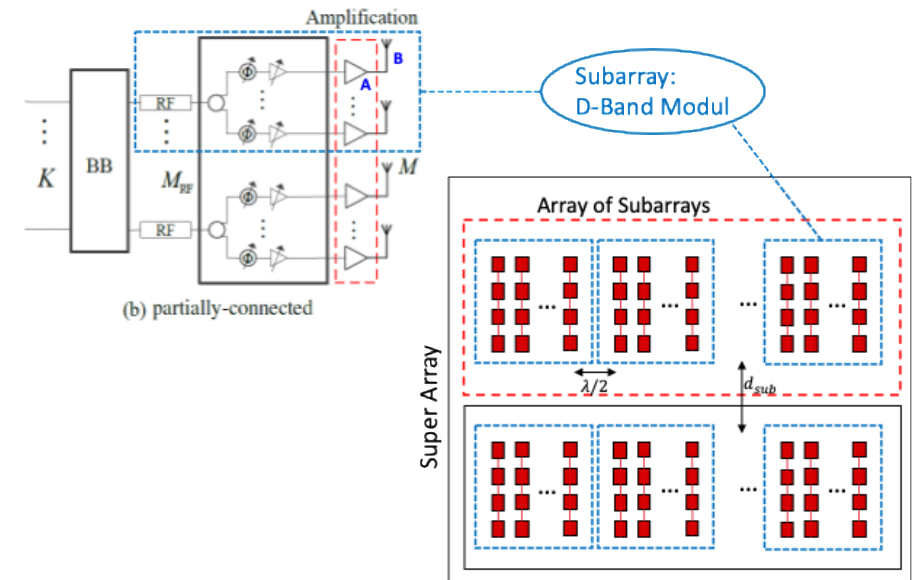
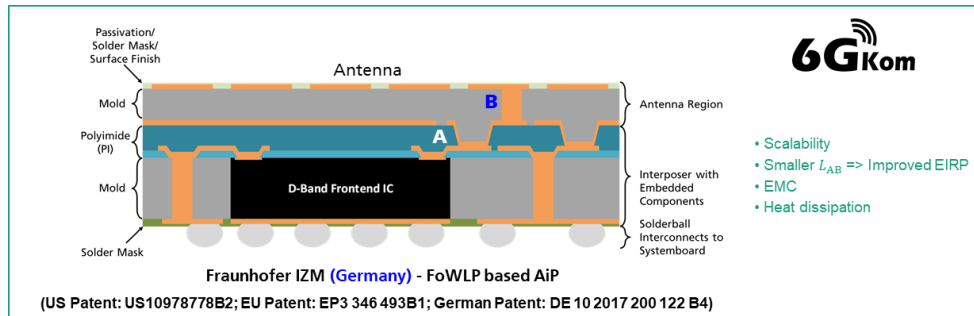
79 GHz automotive radar module






Reliability test

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Example 1: Scalable 6G Sub-THz Module – 1/2

- ❑ Miniaturized D-band front-end module and novel signal processing algorithms for 6G sub-THz
 - ❑ Hybrid-beam forming architecture enables better energy efficiency, scalability and lower HW complexity
- ❑ First 6G sub-THz project funded by German Federal Ministry of Education (BMBF), now BMFTR



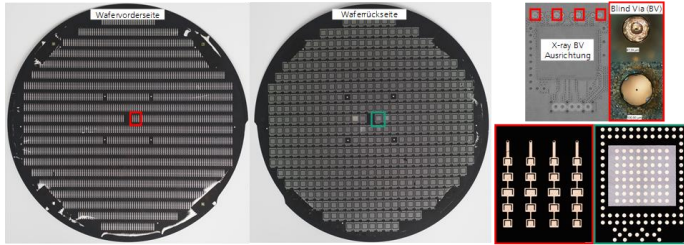
 Technische Universität Berlin	 TECHNISCHE UNIVERSITÄT DRESDEN		 ihp	 Fraunhofer IZM
Prof. Dr. G. Caire	Prof. Dr. G. Fettweis	Prof. Dr. D. Kissinger	Prof. Dr. E. Grass	Prof. Dr. I. Ndip
Competences and Focus				
Information theory and signal processing for mobile communication systems	Signal processing and hardware development for mobile communication systems	Frontend chip design for mmWave and THz systems	Localization, chip development and manufacturing for mmWave and THz systems	Advanced packaging and system integration , reliability, RF system design, signal integrity and antenna design for mmWave and THz systems



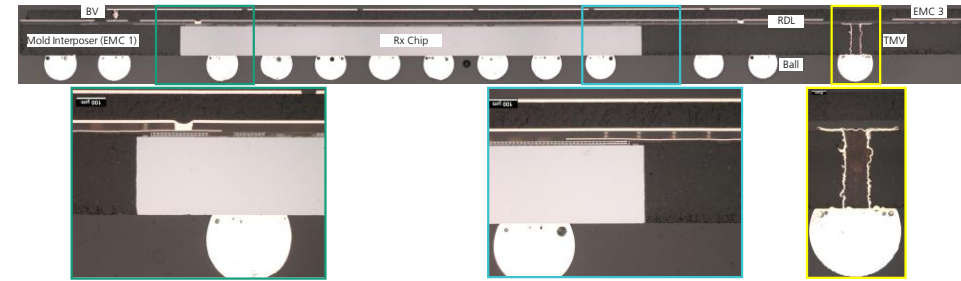
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Example 1: Scalable 6G Sub-THz Module – 2/2

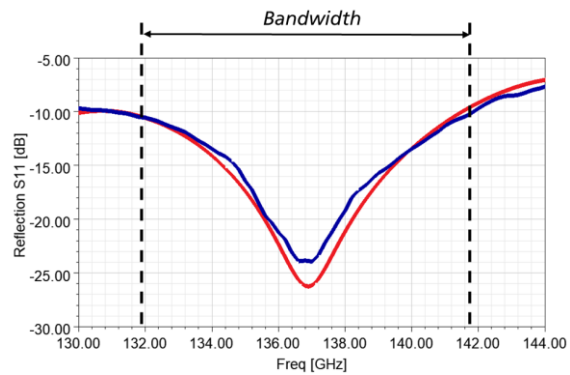
6G THz antenna arrays fabricated at IZM



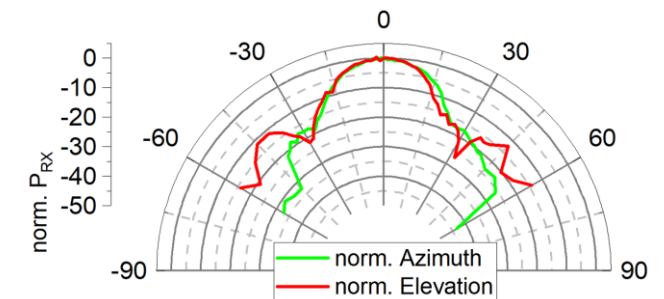
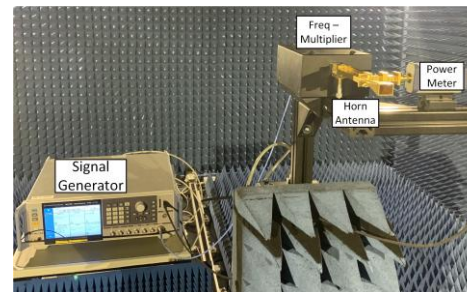
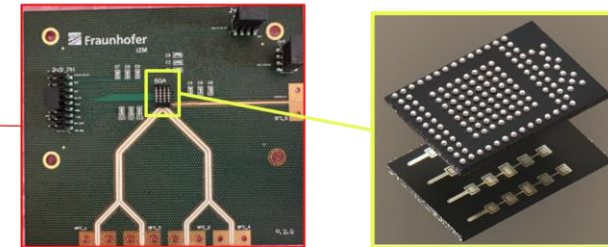
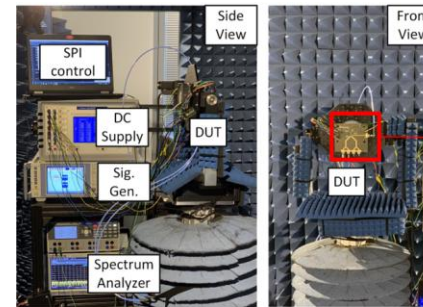
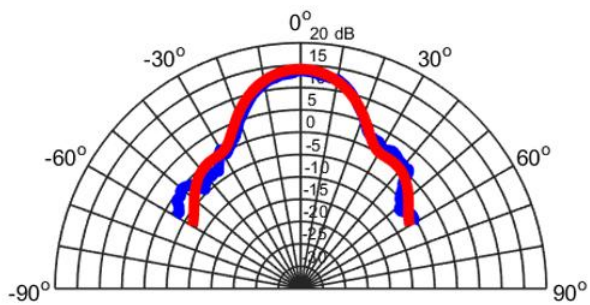
6G THz frontend module fabricated at IZM



6G THz antenna arrays measured at IZM



Measurement █
 Simulation █

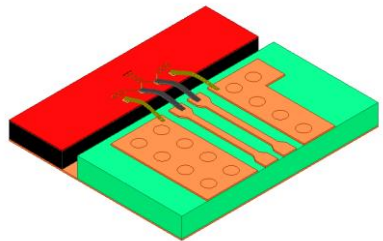
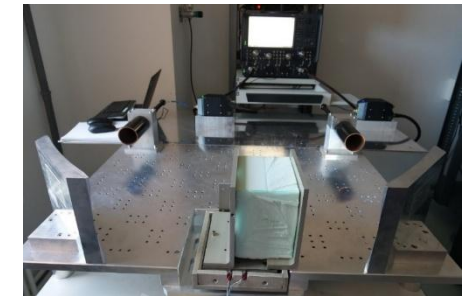


6G THz frontend module measured at IHP

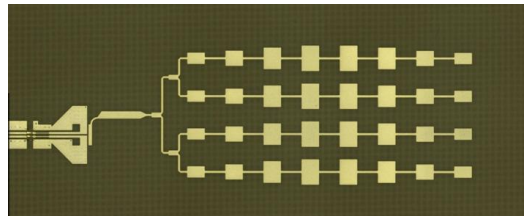
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Example 2: 60 GHz Medical Radar Module – 1/2

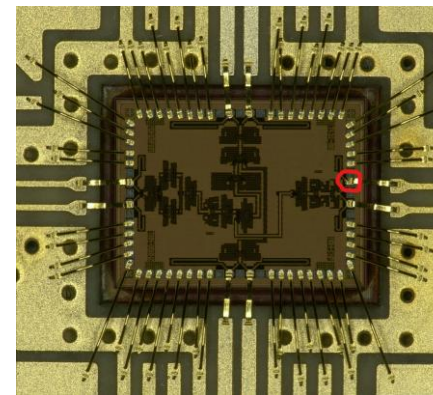
- ❑ **Goal:** Development of low-cost and low-power medical radar system for contactless monitoring of vital signs (breathing, heart rate...)
- ❑ **IZM Tasks:**
 - ❑ Design, fabrication & test of integrated antennas, considering realistic integration environment (housing and bed in hospital environment)
 - ❑ Design of front-end board for integration of radar ICs and antennas
 - ❑ Fabrication of RF front-end board, assembly of radar ICs and housing



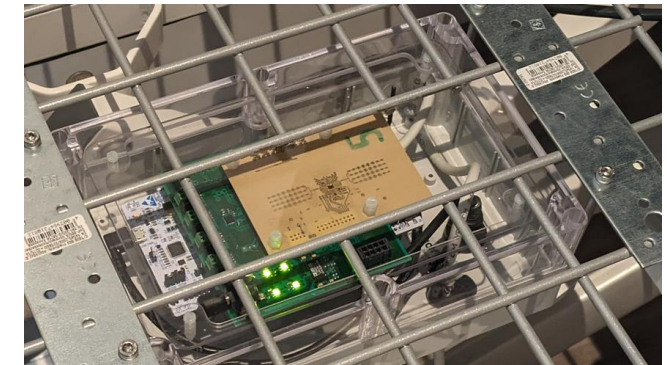
60 GHz wire bonds and compensation structures



60 GHz wire bonds, compensation structures, balun and antenna array



60 GHz wire bonded radar transceiver chip

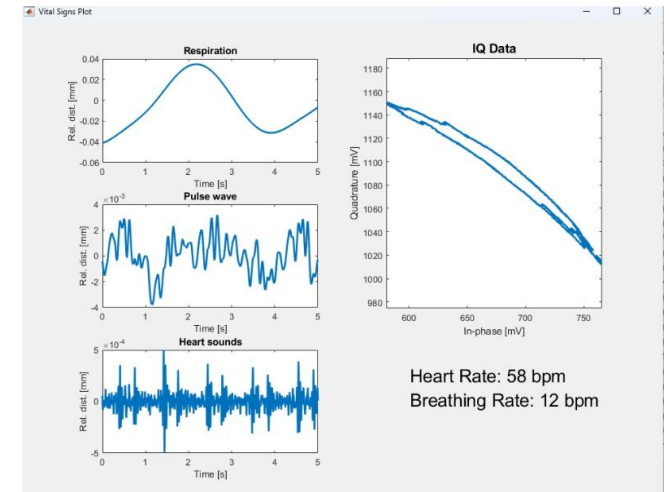
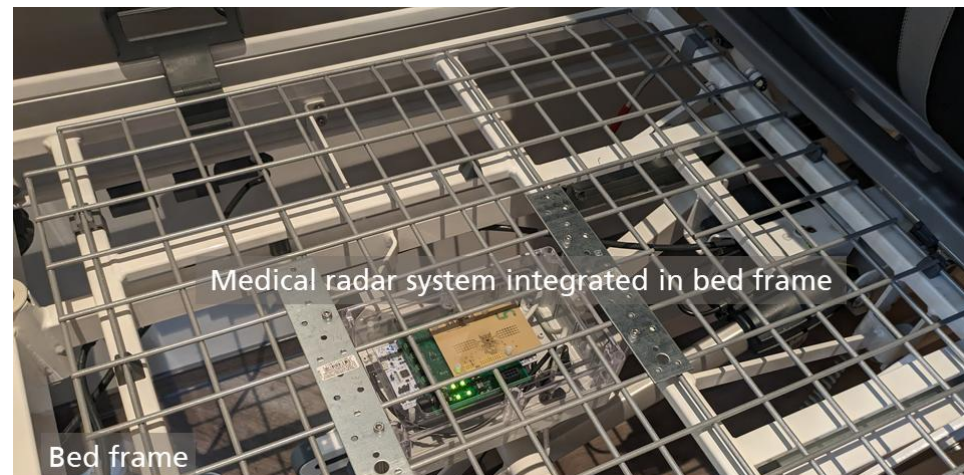
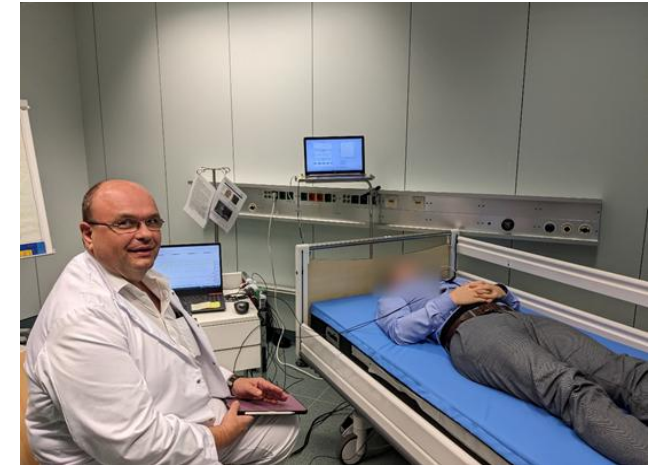


60 GHz medical radar system integrated under patients bed
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Example 2: 60 GHz Medical Radar Module – 2/2

■ Successful Clinical Trials at CTK Hospital Cottbus since 2023

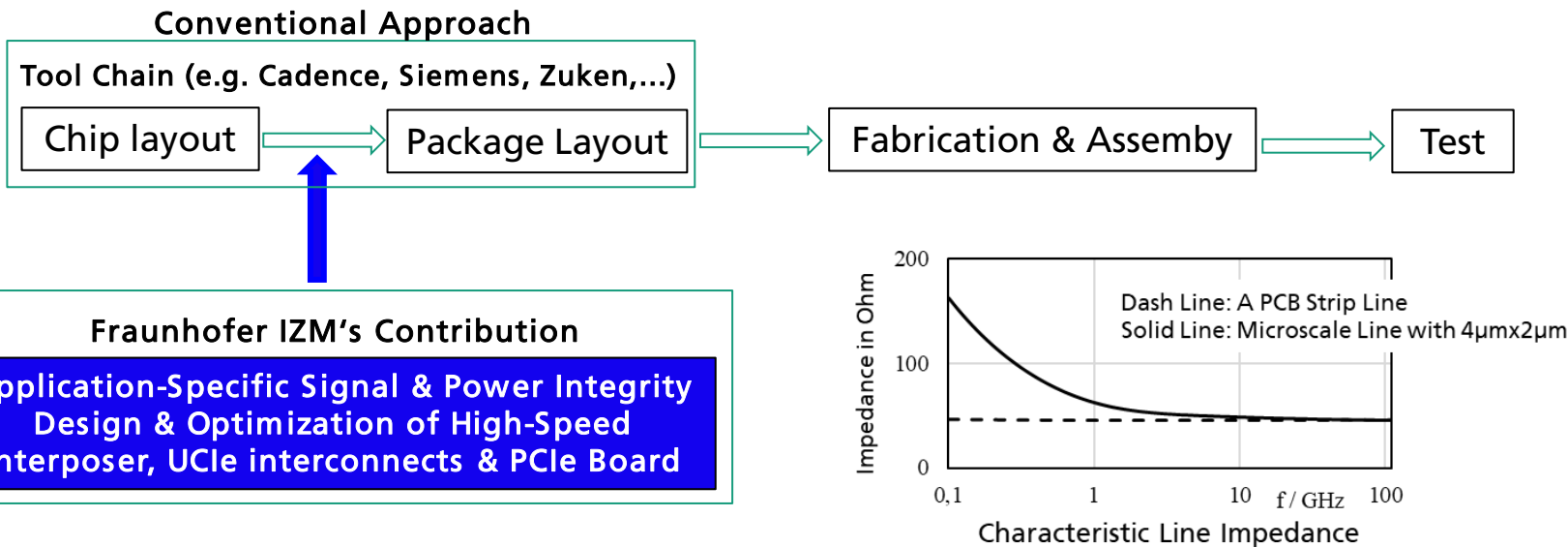
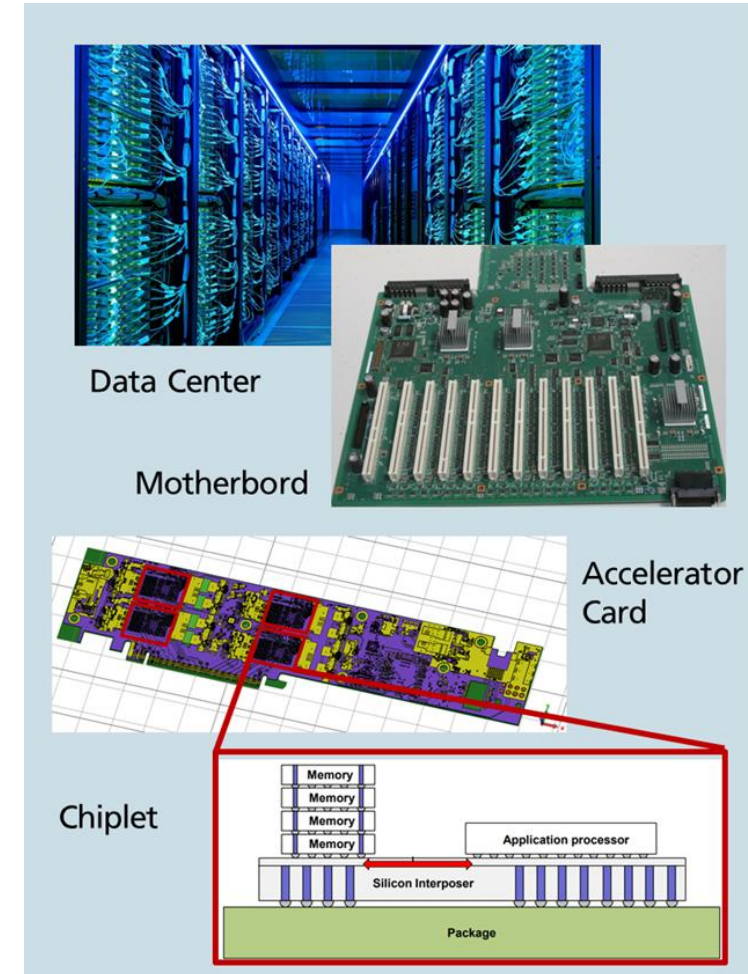
- Medical Radar demonstrator mounted in hospital bed below mattress
- Different subject groups (healthy, with arrhythmias)
- Accurate heart rate and breathing rates measured, lying on back, on side, reading



Medical Radar Analysis GUI

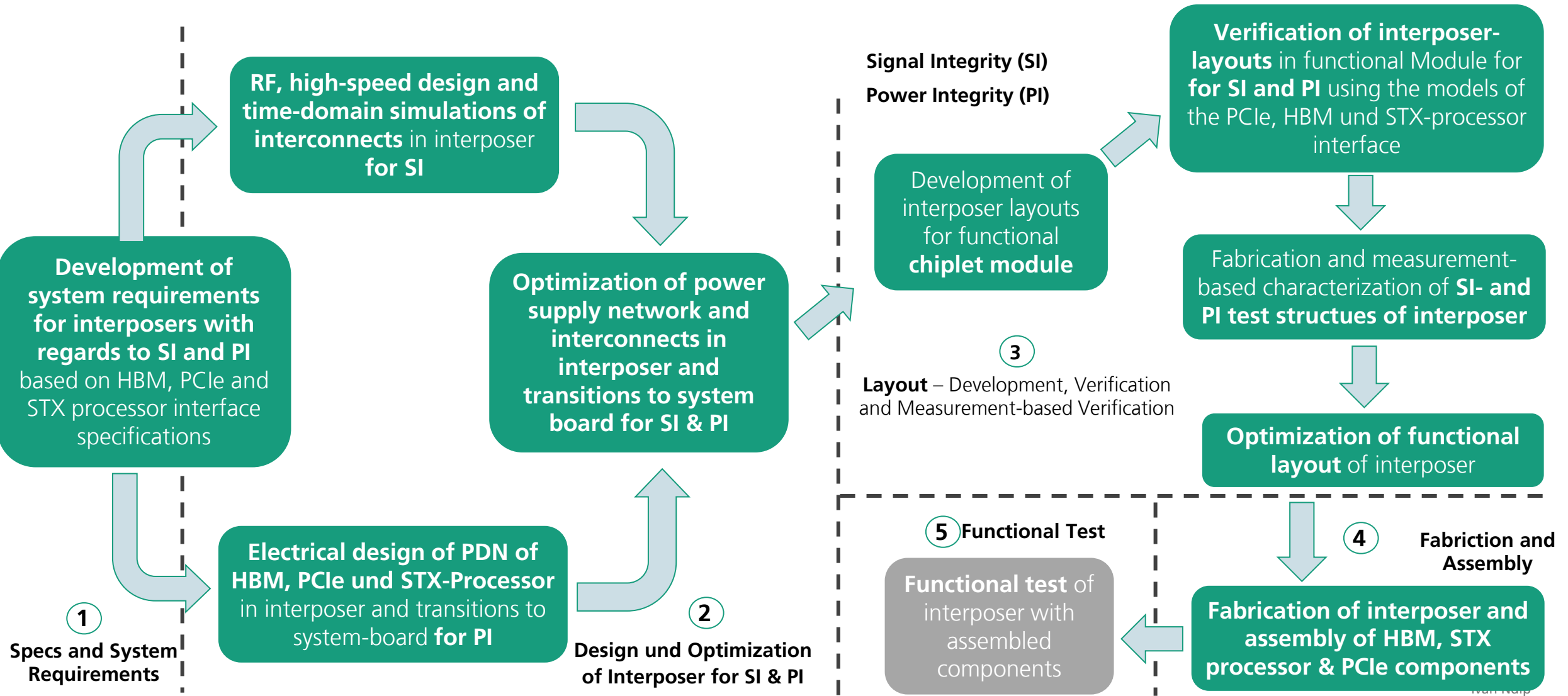
Chiplet Modules for HPC & AI Systems – 1/3

- ❑ **Project Goal:** Development of chiplet module (STX processor and HBM integrated on silicon interposer) as fundamental building block of accelerator cards for HPC & AI applications
- ❑ STX processor architecture (Fraunhofer ITWM), Design of STX processor chip (Fraunhofer IIS); Signal & power integrity design of silicon interposer, fabrication & assembly (Fraunhofer IZM)



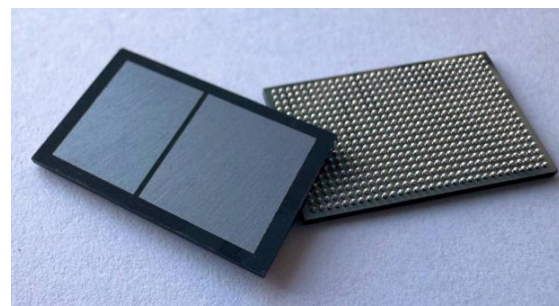
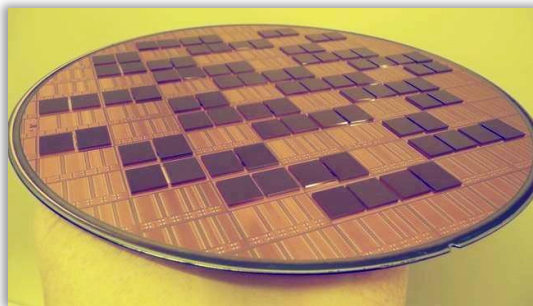
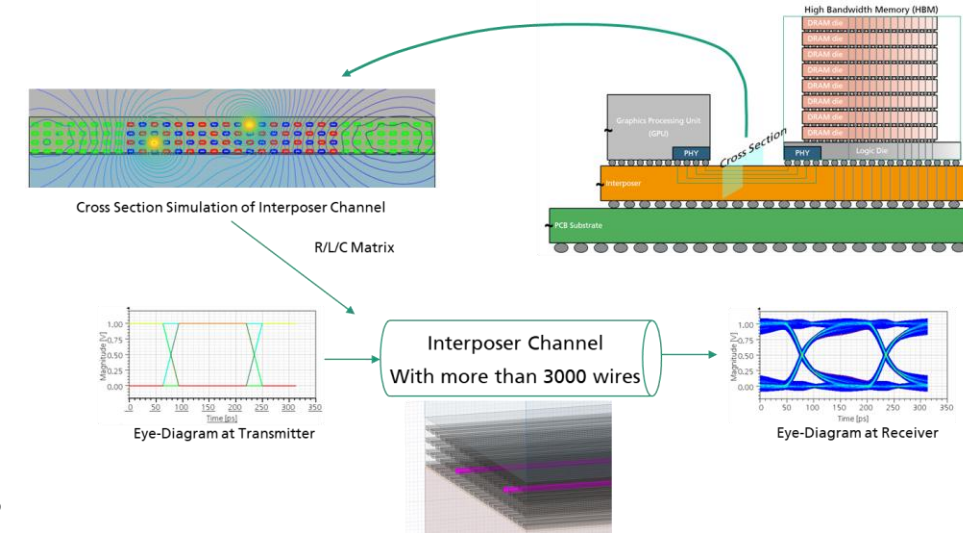
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Chiplet Modules for HPC & AI Systems: IZM Methodology for SI & PI Design – 2/3

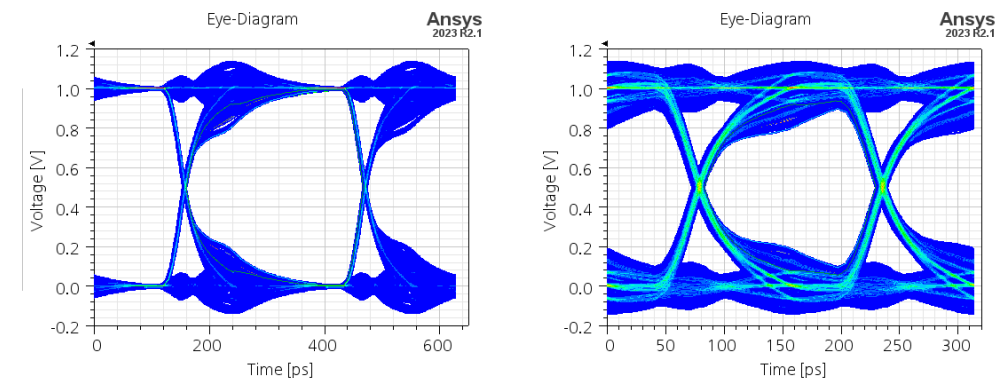


Chiplet Modules for HPC & AI Systems – 3/3

- ❑ System-level signal & power integrity design, layout and fabrication of chiplet module
 - ❑ Silicon interposer with polymer/copper RDL, 4 μm line/space for integration of (STX) processor module and HBM 2e with PCIe Interface (Gen 5)
 - ❑ Size: 250mm²; I/O pin count (840 solder balls, via 300 μm, pitch 660 μm)
 - ❑ Routing > 3000 signal and power lines + 12 different supply voltages
 - ❑ High complexity of PDN
 - ❑ 8 differential high-speed pairs



Samples fabricated at Fraunhofer IZM (WLSI-Berlin)



Measured eye diagrams for data rates corresponding to HBM2e and HBM3

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Key Take Aways

- ❑ Bandwidth drives innovation in radar sensing, communication, HPC & AI applications
- ❑ Bandwidth-related packaging challenges must be addressed for emerging & future applications
- ❑ Fraunhofer IZM provides:
 - ❑ Unique & holistic RF design solutions (from materials to modules) for emerging radar sensing & communication applications
 - ❑ Efficient signal & power integrity design methodology, fabrication & assembly for HPC & AI systems

**Thank you very much for your
attention!**

Contact

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