Performance Comparison of Advanced Power Electronic Packages for Automotive Applications

Sibylle Dieckerhoff¹, Stephan Guttowski², Herbert Reichl¹

1: Technical University of Berlin, Gustav-Meyer-Allee 25, 13355 Berlin
2: Fraunhofer Institute for Reliability and Microintegration, Gustav-Meyer-Allee 25, 13355 Berlin

Abstract: The paper presents an overview over advanced power electronic package solutions for multi-chip modules. To assess their thermal performance, simulation models of the packages are analysed regarding the temperature distribution in the assemblies. The improvement which may be achieved with double-sided cooling of the modules is simulated and compared to the standard chip & wire module. From the simulations, the transient impedance of the chip’s hot-spot is derived and further processed in an automotive case study.

Keywords: power electronic packaging, thermal management, converter design

1. Introduction

Technological improvements in the field of power electronics are driven by automotive applications due to the very challenging requirements regarding volume, power density, costs, reliability and operating temperature. A key issue in this area is the packaging of power electronics forming the limiting factor to performance and reliability of power electronic systems.

In the power and voltage range used in automotive applications, MOSFETs and IGBTs are the state-of-the-art active power devices. They are generally assembled in discrete housing or in power modules. The dice are mounted on DCB substrates or leadframes via large area soldering, and the upper contacts are interconnected via thick wire bond technology. The wire bonds are known to be the main cause of failure of discrete devices under power cycling operations. In power modules additional problems arise from large solder areas. Wire-bonding technology sets structural limits to the integration depth of power electronic systems. Hence, research and industry are currently developing alternative packaging technologies for power electronic semiconductors focusing on higher performance and more flexibility to overall system design. These technologies concentrate on alternatives for the wire bond technology, differing in the method to contact the upper gate and source / emitter pads of the transistors.

Thermal management is a crucial issue as it limits the switching power of converters and has a strong impact on converter reliability due to thermo-mechanical effects in the packages. The focus of this paper is to assess the thermal performance of today’s and of some typical advanced power packaging solutions and to discuss the feasibility for the use in an automotive application.

2. Power Electronic Packages

Figure 1 depicts the assembly of a standard chip & wire (“C&W”) multi-chip power module as described in the introduction. This module represents the reference for the thermal analysis. In the new technologies, the solder interconnects to the bottom DCB and the heat spreader are not modified compared to this standard module.

2.1 Advanced Power Electronic Packages

Several new packaging technologies for power semiconductors have been proposed recently [1-5]. Only a few of them have been commercially realized, e.g. the discrete “DirectFET” by International Rectifier. For multi-chip power modules, solutions to replace the state-of-the-art chip & wire technology may be classified regarding the dimension of the electrical layout. In a 2-dimensional layout, the wire bonds are replaced by alternative interconnection technologies which are supposed to have a higher reliability and / or current carrying capability. Examples are spring contacts, the low temperature joining technique, and solder bumping technologies connecting stripes or small plates of copper to the dice [6-8]. Modules based on a 3-dimensional layout are built as stacked assemblies with a second interconnection layer on top of the devices. The electrical layout is realized either by providing a prestructured circuit board e.g. a flexible substrate or a second DCB that may be soldered to the dice, or by structuring the electrical circuit layout during a planar integration process leading to a multilayer...
assembly. The 3-D-solutions provide the basis either for sensor and control circuitry integration close to the semiconductors within one package or for an improved thermal management due to the double-sided cooling option in case of the availability of a second planar surface.

Typical examples for the 3D-approaches are the planar integration with an Embedded Power Stage by CPES [1], the Planar Power Polymer Packaging Technology by GE [2], the Flip-Chip-on-Flex Technology, also by CPES [3], and the Power-Ball-Grid-Array Technology applying two DCBs by Siemens [4]. A short description of each assembly is given in the following.

Embedded Power ("EP") [1]:
In the embedded power assembly, the dice are embedded into a ceramic frame. The frame is coated with a dielectric in which vias a formed to access the upper source / emitter pads of the transistors and the anode pads of the diodes. By sputtering and electroplating in conjunction with photolithographic processes, a metallization layer is built upon the dielectric forming the electrical interconnects. The thickness of the dielectric is 125µm, the thickness of the metallization is 125-150µms.

Planar Power Polymer Packaging ("P4") [2]:
The "P4" technology proposed by General Electric uses a thin (50µm) polymer film as the upper substrate with vias to connect to the device pads. Metallurgical contacts – by sputtering and electroplating – are formed through these vias and on the upper side of the polymer film. Via diameters for the power pads are 500-1000µm. By electroplating, a copper thickness of 75-125µm is achieved.

Both technologies lack an inherent insulation that would allow a direct contact of the planar surface to a heatsink or heatspreader. Hence, for 2-sided cooling additional insulation measures have to be considered, e.g. applying an intermediate polymer film / dielectric between copper and heatsink or by soldering a DCB on top of the assembly. The latter provides a better thermal performance but counteracts the advantages achieved by using direct metallurgical contacts.

Flip-Chip-on-Flex ("FC-on-Flex") [3]:
The "Flip-Chip-on-Flex" technology is a solder bump technology which uses a flexible carrier for the top interconnect system. Advantages are concerned with the adjustment of heights of different chips and with an expected relaxation of thermomechanical stress.

Double-sided cooling of the flexible carrier poses two principle problems: First, the thermal conductivity of the polymer film is very low. The second problem is due to the fact that the flexible substrate allows for a correction of different chip heights. In consequence, the upper surface cannot be assumed to be sufficiently planar for the direct attach of heatsinks. The double-sided cooling option is thus only analyzed for theoretical comparison purposes.

Power Ball Grid Array ("PBGA") [4]:
In the "PBGA" assembly, the power semiconductors are soldered between two DCBs. While the collector of a die is connected to the lower DCB by large area soldering, the upper gate and emitter pads are connected to the upper DCB via solder bumps. These solder bumps have a diameter between 200 and 250µm. In the example published in [4], variants with 90 to 170 bumps are used to solder MOSFET dice with a size of approximately 4.5x7mm.

A comparable solder technology is e.g. the “Metal Post Interconnected Parallel Plate Structure” assembly presented in [5], where copper posts of different heights are soldered between the dice and the DCBs.
Table 1: Properties and design parameters of the different packaging technologies

<table>
<thead>
<tr>
<th>Interconnect technology</th>
<th>EP</th>
<th>P4</th>
<th>FC-on-Flex</th>
<th>PBGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Top substrate / chip carrier</td>
<td>Sputtering + electroplating</td>
<td>Sputtering + electroplating</td>
<td>Solder bump</td>
<td>Solder bump</td>
</tr>
<tr>
<td>Top metallization</td>
<td>Ceramic (Al$_2$O$_3$) + dielectric (125µm)</td>
<td>Polymer film (50µm)+ adhesive</td>
<td>Flexible polymer (50µm)</td>
<td>2nd DCB</td>
</tr>
<tr>
<td>Top insulation</td>
<td>125µm-150µm</td>
<td>75-125µm</td>
<td>50µm (up to 150µm by loss of flexibility)</td>
<td>typ. 300µm Cu</td>
</tr>
<tr>
<td>Top insulation (prerequisite for 2-sided cooling)</td>
<td>No: additional insulation is required</td>
<td>No: additional insulation is required</td>
<td>Yes: polymer - low thermal conductivity - no planar surface</td>
<td>Yes: 2nd DCB - good thermal conductivity - planar surface</td>
</tr>
<tr>
<td>Material parameters</td>
<td>- Ceramic (AlN, Al$_2$O$_3$) - Dielectric</td>
<td>- Polymer - Underfill</td>
<td>- Solder - Underfill</td>
<td>- Solder - DCB</td>
</tr>
<tr>
<td>Geometry parameters</td>
<td>- Metallization - Chip contact area</td>
<td>- Metallization - Chip contact area</td>
<td>- Flex metallization - Diameter, height and pitch of bumps</td>
<td>- Diameter, height and pitch of bumps</td>
</tr>
<tr>
<td>Height adjustment of chips</td>
<td>Add. Cu shims</td>
<td>Flexible carrier</td>
<td>Flexible carrier</td>
<td>Add. Cu shims</td>
</tr>
</tbody>
</table>

2.2 Design parameters

Package design parameters include materials, geometries and the choice of semiconductor chips (size, thickness) to be packaged. The following list summarizes the basic geometry data for all assemblies:

- Standard DCB substrate:
  - Footprint 30mm x 25mm
  - Al$_2$O$_3$ ceramic
  - Layer: 300µm Cu – 380µm Al$_2$O$_3$ – 300µm Cu
- Baseplate: 3mm Cu
- Solder interconnects: 100µm thickness
- MOSFET / IGBT and diode chips assuming square chips with 4, 6, 8 and 10 mm chip length and a thickness of 175µm.
- The possible contact area of the top source / collector pads varies from 30% to 80% of the chip area.

Typical material parameters - thermal conductivity, specific heat, density - were taken from the literature (see appendix).

3. Basic Thermal Characteristics of the Packages

Losses in the power modules arise in the power devices but also as ohmic losses in the substrate and the interconnects, e.g. in the wire bonds or in the copper metallization areas of the multilayer packages, posing demands on metal thickness. In the first step, only losses in the semiconductors are considered, as the ohmic losses depend on the individual electrical layout of the packages. The wire bond technology limits cooling to the one-dimensional heat-flow to the baseplate or to a directly attached heatsink. The potential for double-sided cooling is often referred to as a benefit of the 3-D “sandwich” packages. To assess the achievable improvement in output power, the assemblies are simulated assuming single- and double-sided cooling. All thermal simulations are conducted with the commercially available software tool “Flotherm”.

3.1 Simulation models

For the semiconductor hot-spot, the steady-state thermal resistance $R_{th}$ and the transient thermal impedance $Z_{th}$ are derived via simulation of the temperature distribution within the packages. To reasonably limit the degrees of freedom of the package design, a simple basic simulation model with only a single die is defined. Very good heat spreading is imposed by choosing the substrates and heat sinks sufficiently large. To decouple the package analysis from the individual cooling system, the thermal impedances case-to-heatsink and heatsink-to-ambient were not modeled. The simplest approach defines a constant temperature at the bottom of the heat spreader which allows to concentrate on the mechanisms of heat conduction within the packages. Figure 6 depicts the basic model, figure 7 shows the commonly used impedance networks to describe the thermal path

---

1. To account for the thermal coupling of several semiconductor chips in multi-chip modules, superposition of the resulting impedance networks is required.
from the heat source in the chip down to the heatsink.

The temperature rise at the chip is a function of the power loss $P(t)$ and calculated from the model in figure 7b with typically $n=4$:

$$T_j = T_{case} + P_i(t) \cdot \sum_{i=1}^{n} R_i \cdot \left(1 - e^{-t/R_iC_i}\right)$$  \[1\]

To handle the measured or simulated $Z_{th}$-curves, the $R_i$, $C_i$ parameters of the partial fraction model are determined by numerical curve fitting.

3.2 Reference measurement

To verify the basic geometry and material parameters of the simulation, the steady-state and the transient thermal impedance of a standard 1200V IGBT module are measured and compared to the simulation model. In compliance with JEDEC standard JESD24-12, first, a calibration curve relating the device on-state voltage to the device temperature is recorded using a small constant measurement current and external heating. In the second step, a current pulse is applied and the decay of the device voltage at the falling edge of the pulse is measured. The temperature of the heatsink is kept constant and forms the reference temperature of the setup. Hence, the measured thermal path includes the module baseplate and the thermal grease (1W/mK, ~100µm) which must be considered in the simulation of the reference model. Figure 8 shows the measured thermal impedance in comparison to the simulation data. Good agreement between simulation and experimental results is achieved for pulse times above 1ms. The dynamics of the measurement setup was not sufficient to measure correctly in the µs range. Furthermore, the deviation at the end of the pulse is due to inaccuracy in modeling the thermal grease interface.

3.3 Simulation of thermal package characteristics

Single-sided cooling:

Each of the considered package technologies has been modeled according to the example in figure 6. Varying the chip size, a parametric study has been performed to identify the steady-state thermal resistance $R_{th} = \Delta T / P_{chip}$ and the transient thermal impedance $Z_{th}(t) = \Delta T / P_{chip}(t)$ of the hot-spot in the chip. In figure 9, the steady-state simulation results for the standard C&W module are compared to the calculated resistance ($d_i$: thickness layer $i$, $a_i$: chip length, $A=a^2$ chip area; $\alpha_i$=45° heat spreading angle):

$$R_{th} = \sum_i \frac{d_i}{\lambda_i \cdot (a_i + d_i \tan \alpha_i)} = \sum_i \frac{d_i}{\lambda_i \cdot (a_i + d_i)}$$  \[2\]

Due to the effect of heat spreading and the accumulation of heat in the chip center especially of large chips, the steady-state resistances are not linearly related to the chip size and deviate from the simulation results. The basic time constants, however, are comparable for the different chip sizes, as heat spreading affects the thermal resistance and the thermal capacitance (figure 9). Figure 10
compares the transient impedance $Z_{th}$ of the different packages for the 8mm chip. Figure 11 contains the simulated impedances for all the new packages.

Due to the large metallization surface in the new packages, parallel heat paths from the metallization through the insulation to the bottom DCB via polymer/soft encapsulation/ceramic exist. The thermal conductivity of the insulation materials is very low, which limits the achievable reduction of the total resistance in the parallel impedance network.

Figure 12: Heat paths in a sandwich assembly

Table 2 gives the average improvement of the steady state resistance $\Delta R_{th}$ (in %) of the new packages compared to the standard module. The contact area on the top of the chips is also a relevant degree of freedom in the design. A total of 30% contact between top substrate and chip (metallurgical or solder) is typical for the assemblies described in references [1-4]. Restrictions from the chip layout (e.g. gate pads) limit the maximum contact area to approximately 80%.

<table>
<thead>
<tr>
<th></th>
<th>C&amp;W</th>
<th>EP</th>
<th>P4</th>
<th>FC Flex</th>
<th>PBGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_c=30%$</td>
<td>-</td>
<td>8%</td>
<td>5%</td>
<td>7%</td>
<td>11%</td>
</tr>
<tr>
<td>$A_c=80%$</td>
<td>-</td>
<td>11%</td>
<td>7%</td>
<td>8%</td>
<td>14%</td>
</tr>
</tbody>
</table>

Table 2: Improvement of thermal resistance $R_{th}$ in % (8mm chip, $A_c$: contact area)

The PBGA assembly has a good heat distribution in the DCB layers and a minimum distance between top and bottom DCB. This leads to the comparably best results. The impact of the ceramic carrier in the embedded power module is low, because the dielectric (thickness of 125µm [1]) governs the thermal resistance. All values summarized in table 2 represent an optimum: in multichip-modules, the electrical layout will reduce the effective top metallization area.

The results make clear that with single-sided cooling, no significant performance improvement is achieved with the new packages due to the low thermal conductivity of intermediate materials like the soft encapsulation or the dielectrics. A possible option could be to include additional thermal vias between top and bottom substrate. However, this will increase the footprint of the package, because additional space on the bottom DCB is needed for electrical insulation reasons.

**Double-sided cooling**

The same parameter studies have been conducted with a simulation model applying double-sided cooling. To limit the discussion to package properties, again a basic model with a second baseplate is chosen, with the same constant temperature for both heatsinks (figure 13). For the
P4 and the EP assemblies, which have no inherent electrical insulation, an insulation foil (50µm) is applied on top of the metallization. The variant to solder a second DCB upon the metallization was not considered.

Figure 13: Thermal model (PBGA), 2-sided cooling

![Figure 13: Thermal model (PBGA), 2-sided cooling](image)

Figure 14: $Z_{th}$ comparison (8mm die), 2-sided cooling

![Figure 14: $Z_{th}$ comparison (8mm die), 2-sided cooling](image)

Figure 15: Parallel heat paths to the 2$^{nd}$ heatsink²

![Figure 15: Parallel heat paths to the 2$^{nd}$ heatsink²](image)

Figure 16: $Z_{th}$-Comparison 2-sided cooling to 1-sided cooling (dashed lines), 8mm chip

![Figure 16: $Z_{th}$-Comparison 2-sided cooling to 1-sided cooling (dashed lines), 8mm chip](image)

In a complete system model, the thermal impedances to same ambient need to be modeled instead of using two constant temperature sources.

### 4. Automotive Application Example

Power electronics for automotive applications include different types of voltage source converters as well as different controllers with linear operation of semiconductors. The half-bridge converter forms a fundamental building block for 3-phase motor converters, H-bridge configurations for motors and bidirectional DC/DC converters as well as buck converters e.g. for future 42V to 14V DC/DC conversion. The following case study will exemplarily relate the design of a three-phase motor converter to the packaging technologies discussed in section 3.

#### 4.1 Case study: converter for HEVs

Today’s electric motor solutions for HEVs are either induction motors or permanent magnet synchronous motors. For the European market, a rated electric motor power is typically 50kW. The motors are controlled with three-pulse IGBT converters. The converters may either be connected directly to the

<table>
<thead>
<tr>
<th>$A_c$: contact area</th>
<th>C&amp;W</th>
<th>EP</th>
<th>P4</th>
<th>FC Flex</th>
<th>PBGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_c=30%$</td>
<td></td>
<td>14%</td>
<td>12%</td>
<td>14%</td>
<td>31%</td>
</tr>
<tr>
<td>$A_c=80%$</td>
<td></td>
<td>18%</td>
<td>15%</td>
<td>17%</td>
<td>44%</td>
</tr>
</tbody>
</table>

Table 3: $R_{th}$ improvement due to 2-sided cooling compared to the C&W module ($A_c$: contact area)

² In a complete system model, the thermal impedances to same ambient need to be modeled instead of using two constant temperature sources.
battery \((U_{\text{Bat}} = 300V \pm 20\%\) or to a higher constant dc-link voltage which is generated by an additional bi-directional boost converter (e.g. 650V in the Toyota Lexus vehicle). For direct operation from the battery, feasible semiconductors are IGBTs and diodes with a standard blocking voltage of 600V. Cooling option is liquid cooling with a coolant temperature of 85°C plus overshooting.

![Basic converter topology](image)

**Figure 17: Basic converter topology**

Crucial for the semiconductor losses and hence for the heat generation is the output current \(I_{\text{rms}}\). Assuming a space vector modulation scheme for the converter and a typical induction motor with \(\cos \phi = 0.85\), the rated current \(I_{\text{rms, rated}}\) calculates to 200A \((P=50kW, U_{\text{Bat}}=240V)\). The operating point which determines the converter design is the motor start. Here, currents up to 1.5-2 times the rated current are required for several seconds. For induction motors, the minimum frequency is the slip frequency of 1-2Hz which gives a significant temperature swing with the momentaneous power loss related to the current.

For the study, loss parameters for standard 600V IGBTs and diodes are taken from the datasheets \([9]\) and scaled to the chip area\(^3\). Rated current densities of the IGBTs are approximately 2A/mm\(^2\) (total chip size), the size of the diode is generally 50% of the IGBT size. In accordance to today's standard, a switching frequency of 8kHz is chosen, being sufficient for control requirements and well above noise level. The rms current is set to the rated chip current, and with a numerical calculation program based on \([10]\), the average IGBT losses in the critical operation point are calculated to \(P_{\text{av}} = 1.2W/mm^2\). To evaluate the temperature rise at the chip, the momentaneous power loss is applied to the \(Z_{\text{th}}\)-value of the packaged chip. The latter is derived by curve fitting from the simulation results presented in the preceding section.

4.2 Simulation results

Figure 18 compares the temperature rise at the IGBT junction for the C&W standard module, the PBGA module with double-sided cooling and the EP module, also applying double-sided cooling. The response of the P4 and the FC-on-flex modules are comparable to the EP assembly and not depicted here. The simulations show that in the standard C&W modules, the current loading of the chips must be reduced, i.e. more chip area is needed, because the maximum IGBT junction temperature is above the rating. Furthermore, it can be deduced that

- for a reliable estimate of the expected chip temperature, the \(Z_{\text{th}}\) value has to be related to the momentaneous power loss;
- as the time constants of the \(Z_{\text{th}}\) curves for the different packages are comparable, the relative reduction in junction temperature is proportional to the relative improvement in the \(R_{\text{th}}\) which is up to 40% for the PBGA assembly. Slightly reduced - to account for \(R_{\text{th}}\) variations with the chip size and also considering thermal coupling of paralleled chips in real assemblies - this can be used for a reduction of the required silicon in a comparable magnitude.

![Temperature swing at the IGBT hot spot](image)

**Figure 18: Temperature swing at the IGBT hot spot; converter operation at 2Hz output current frequency**

<table>
<thead>
<tr>
<th>(\Delta T) ((Z_{\text{th}}) simulation)</th>
<th>C&amp;W</th>
<th>EP</th>
<th>PBGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>(\Delta T_{\text{av}} = P_{\text{av}} R_{\text{th}})</td>
<td>77K</td>
<td>60K</td>
<td>44K</td>
</tr>
</tbody>
</table>

**Table 4: Maximum simulated temperature rise \(\Delta T\) at the IGBT compared to the average temperature rise**

5. Summary

In this paper, several recently proposed packaging technologies for IGBT or MOSFET power modules have been investigated regarding their thermal performance. For the analysis, simulation models of the packages were implemented in a commercial software tool. From the temperature distribution within the packages, the relevant thermal property - the thermal impedance - was derived assuming single- and double-sided cooling of the assemblies.
The results show that the “PBGA” technology provides the best basis for a higher silicon utilization compared to standard modules. Theoretical values up to 40% were calculated using double-sided cooling concepts. If the insulation to the second heatsink is not realized by ceramic materials, as it was the case in the other investigated technologies, the possible improvement falls to 15%.

6. References


7. Appendix

<table>
<thead>
<tr>
<th></th>
<th>( \lambda ) [W/m K]</th>
<th>( c ) [J/kg K]</th>
<th>( \rho ) [kg/m³]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon</td>
<td>120</td>
<td>700</td>
<td>2330</td>
</tr>
<tr>
<td>Solder (PbSn)</td>
<td>50</td>
<td>150</td>
<td>8400</td>
</tr>
<tr>
<td>Copper</td>
<td>385</td>
<td>385</td>
<td>8930</td>
</tr>
<tr>
<td>Alumina</td>
<td>22</td>
<td>880</td>
<td>3720</td>
</tr>
<tr>
<td>AlN</td>
<td>170</td>
<td>725</td>
<td>3300</td>
</tr>
<tr>
<td>Polymid</td>
<td>0.2</td>
<td>1100</td>
<td>1400</td>
</tr>
<tr>
<td>Dielectric layer</td>
<td>0.3</td>
<td>1400</td>
<td>1120</td>
</tr>
<tr>
<td>Encapsulation</td>
<td>0.5⁴</td>
<td>-</td>
<td>1400..3900</td>
</tr>
</tbody>
</table>

Table 5: Summary of material properties

8. Acknowledgement

The authors would like to thank Dr. Bernhard Wunderle for the valuable discussions.

⁴ Conservative estimate