

PRESS RELEASE

PRESS RELEASEAugust 18, 2021 || Page 1 | 4

Panel Level Packaging Consortium 2.0 – The First Year!

Despite the COVID-19 crisis, Fraunhofer IZM and its 17 partners on the PLC 2.0 consortium have achieved excellent results within the first year. All partners met in a virtual meeting for two days. The time difference for such world-wide meetings is a challenge, therefore several sessions have taken place over the whole day to have easy access from Asia, Europe and the US.

In 2016, Fraunhofer IZM teamed up with a group of industry leaders from Europe, the US, and Japan to develop the fundamental processes for new panel level packaging technologies that are ready to transition to industrial-scale high-volume production. The first incarnation of Panel Level Packaging Consortium (2016 – 2019) consisted of 17 international partners from industry and was judged to be a high-powered and impactful project, having a recognized expert for substrate technologies and wafer-level packaging at its helm in the form of the Fraunhofer Institute of Reliability and Microintegration. For its first run, the focus of the consortium was on the entire process chain in panel-level packaging: from assembly, molding, wiring, and cost modelling to standardization.

With the second consortium launched for 2020 – 2022, this focus has shifted to die placement and embedding technology for ultra-fine-line wiring down to 2 µm lines and space with a potential move to 1 µm. As such, migration effects and ways to exploit the migration limits of fine line wiring have become areas of interest for the consortium's international members, including another 17 partners from industry: Ajinomoto Fine-Techno Co., Amkor Technology, ASM Pacific Technology Ltd., AT&S Austria Technologie & Systemtechnik AG, Atotech, BASF, Corning Research & Development Corporation, Dupont, Evatec AG, FUJIFILM Electronic Materials U.S.A., Intel Corporation, Meltex Inc., Nagase ChemteX Corporation, RENA Technologies GmbH, Schmoll Maschinen, Showa Denko Materials Co. Ltd (former Hitachi Chemical Company, Ltd), and Semsysco GmbH.

The PLC 2.0 project has again made excellent progress: New equipment for panel level packaging had been installed during the run-up to the PLC 2.0, and the project benefits from several major investments made by the German Federal Ministry of Education and Research to promote the Research Fab Microelectronics Germany. The impact of the global COVID-19 pandemic and the subsequent lockdown restricted access to laboratory work and to the research network of the Fraunhofer IZM, leading to the work plan for the PLC2.0 being extended by 4 months. All meetings of the first year were organized in virtual format with two dedicated sessions for the relevant Asia and US time zones.

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One major focus of the project has been the investigation of warpage and die shift in large format reconfigured panels (18" x 24"), and considerable progress has already been made towards understanding the root causes. With these insights, the relevant parameters can now be controlled better to enable large-area fine-line RDL processes. The analytical effort has paid off, as RDL could be scaled down considerably on the panel level, making the most of the advantages of both wafer and panel-level technologies and paving the way for an entirely new process chain with new equipment and materials.

PRESS RELEASEAugust 18, 2021 || Page 2 | 4

Building on this achievement, the consortium's partners are now expecting twelve months of agile progress with developing and managing viable process options on the road to a complete high-yield process chain. The test structures for electrochemical migration tests were also designed in accordance with the IPC standard; the design of the test vehicles was guided by the standard's description of the IPC multi-purpose test board, but with the structure sizes matched to the geometries reflecting the goals of the PLC2.0 project as interdigital structures. Researching a combination of economic and environmental assessments to promote more sustainable production approaches is another strong part of the PLC 2.0. A first model to estimate the carbon footprint of the PLP technology has already been established. This first calculation will help all members to identify the most energy intensive stages and further improve the data quality in the most relevant steps.

Tanja Braun, Group Leader at Fraunhofer IZM, is the public face of the Panel Level Consortium

"What makes me happy about our work is seeing such a diverse consortium coming together and making progress towards one shared goal: Finding future manufacturing technologies for maximum integration density on the panel level."

(Text: Tanja Braun, Michael Töpfer)

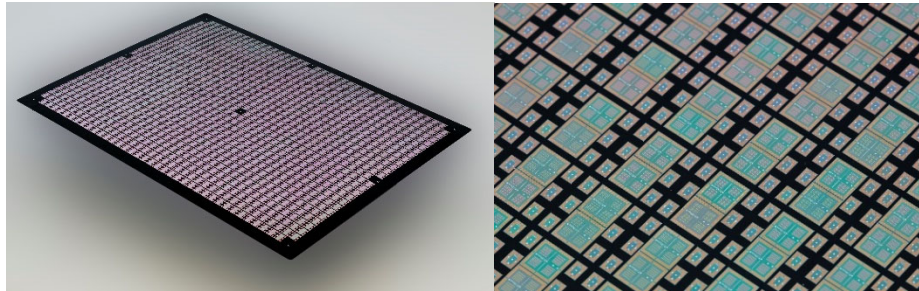
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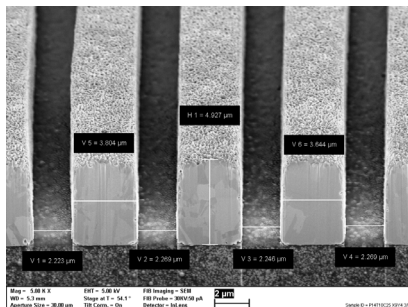
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First results of PLC 2.0: Fully populated panel with embedded chips (left); detailed view (right)

PRESS RELEASE

August 18, 2021 || Page 3 | 4



FIB cut of an ultrafine line wiring layer on panel size (pitch: 5 μm)

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