Fraunhofer IZM

Fraunhofer Institute for Reliability and Microintegration IZM

Department

Wafer Level System Integration – ASSID
All Silicon System Integration Dresden

All Silicon System Integration Dresden – Fraunhofer IZM-ASSID

Fraunhofer IZM

The Fraunhofer Institute for Reliability and Microintegration IZM is one of 75 Fraunhofer institutes conducting contract research for customers from industry and the public sector in Germany. The Fraunhofer-Gesellschaft is the leading organization for applied research in Europe. Fraunhofer IZM is a worldwide renowned institute specialized in the development of advanced packaging and system integration technologies, which are then transferred to industry. The institute is thus able to offer customer-specific solutions for microelectronic products in the overall scope of smart system integration.

» Bringing excellence of 3D heterogeneous integration to the leading-edge industry

Fraunhofer IZM – ASSID

Fraunhofer IZM's center "All Silicon System Integration Dresden – ASSID" operates a leading-edge, industry-compatible 200/300 mm 3D wafer-level process line (ISO 9001-15) with modules for TSV formation, pre-assembly (thinning, singulation), wafer-level assembly and stack formation. ASSID focuses on process development, material and equipment evaluation as well as R&D services and prototyping for small to mid-size volume manufacturing. It is a partner in national, European and worldwide industrial and scientific projects and networks for 3D system integration, e. g. European Chips Act, European ECA pilot line "Advanced Heterogeneous System Integration", PREVAIL, Tech-for-Trust" T4T, QSolid, SEMECO and the Silicon Saxony Network. Fraunhofer IZM-ASSID has established cooperation and joint development programs with industrial partners for undertaking material and equipment evaluation, process development as well as process product integration. Fraunhofer IZM is a member of the FMD – "Research Fab Microelectronics Germany" (www.forschungsfabrik-mikroelektronik.de)

Cooperation Activities

Within the realms of academia, IZM-ASSID is cooperating with

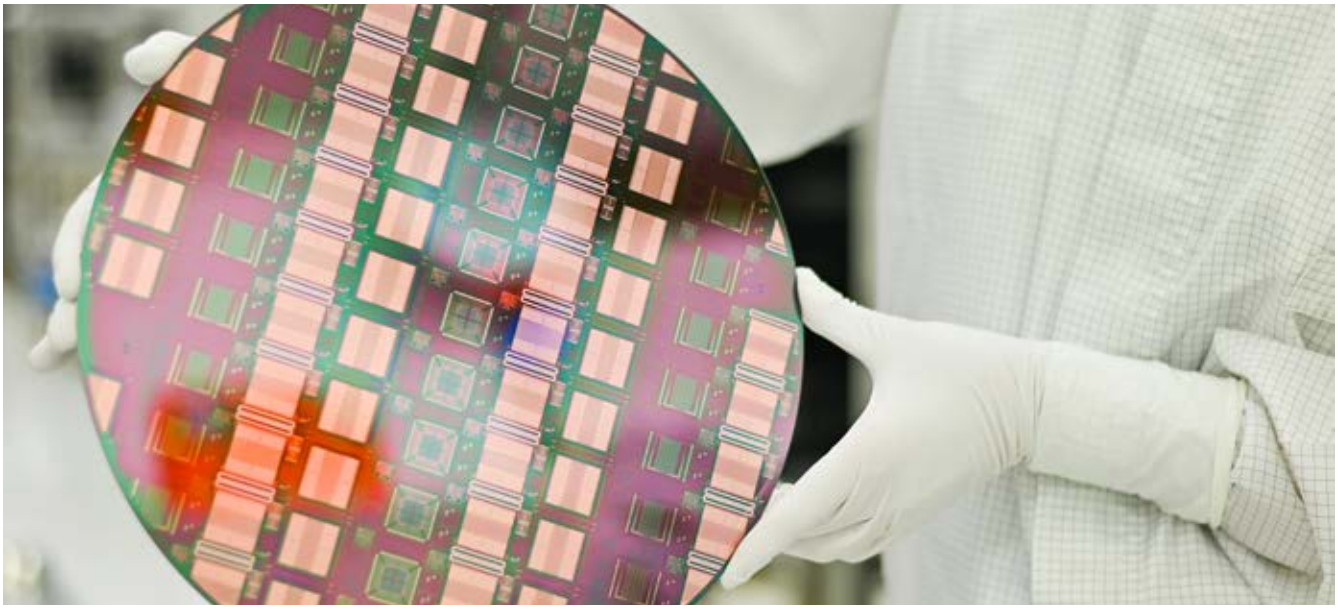
- Technische Universität Dresden (Electronic Packaging Laboratory, IAVT)
- Technische Universität Berlin
- Technische Universität Chemnitz
- Brandenburg University of Technology
- International research labs in Europe, USA and Asia

Fraunhofer IZM, IIS-EAS, IPMS, ENAS, TU Dresden, TU Chemnitz and Dresden University of Applied Sciences cluster with excellence in the fields of micro / nano electronics are strengthening the competitive and innovative capacity of the Free State of Saxony. Research know-how accompanied with resident companies enables faster implementation of innovations in applications and products:

Center for Advanced CMOS and Heterointegration Saxony (CEASAX):
Research platform for 300 mm Frontend and Backend Wafer Level Integration, with access to the most advanced technologies – from developing new IP up to pilot fabrication! (www.cmos-center.com)

Chiplet Center of Excellence (CCoE):
Unique research activity on broad portfolio in design, implementation and test of 2.5 and 3D integrated electronic systems. (www.chiplet-center.fraunhofer.de)

High Performance Center »Functional Integration in Micro- and Nanoelectronics« (Center Micro/Nano):
A special platform across the participating institutes with competences in systems design, components and related fabrication technologies, as well as systems integration. (www.leistungszentrum-mikronano.de)

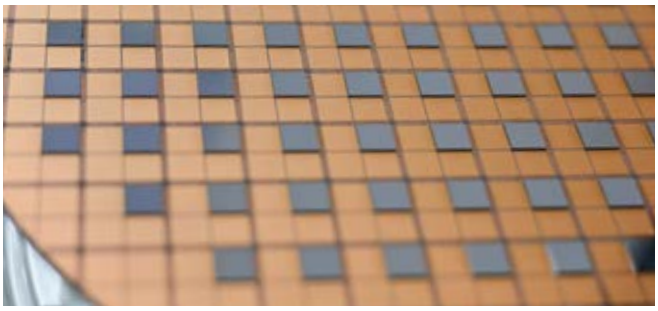


Heterogeneous 3D Wafer-Level System Integration

3D integration is crucial for future innovative products, enabling high performance, compact form factors, and enhanced functionality in fields like ICT, security, healthcare, mobility, transportation, industrial electronics and quantum computing. It integrates multiple devices, such as sensors, MPUs, ASICs, and transceivers, into optimized wafer-level system-in-packages (WL-SiPs). This requires 3D heterogeneous integration technology, a key driver in advanced electronic packaging.

3D Wafer-level System in Package

Fraunhofer IZM-ASSID offers prototyping and low-volume manufacturing (300/200 mm) at its advanced wafer-level packaging pilot line certified according ISO 9001-15. Fraunhofer IZM-ASSID has established strong cooperation with leading material and equipment suppliers in which customer-specific solutions in the fields of material, equipment and processes are developed and introduced into products. Fraunhofer IZM-ASSID provides comprehensive 3D integration support, including design, technology, and reliability, in partnership with Fraunhofer institutes and established unique research platforms.

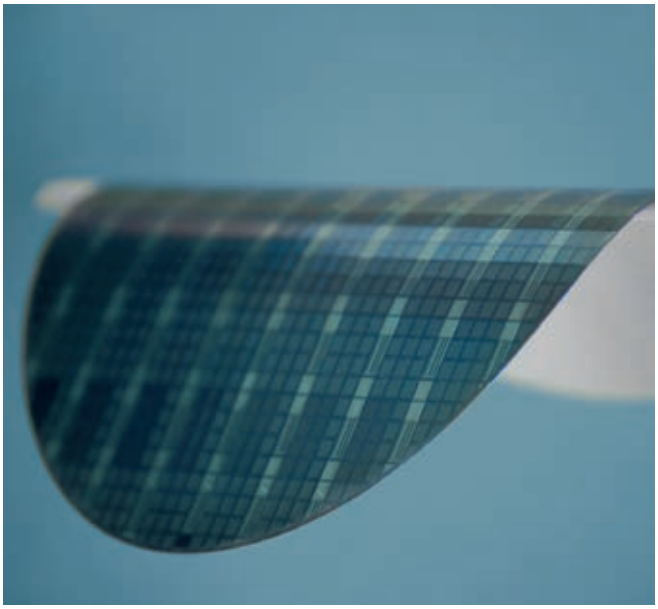


Core Competencies and Technological Services:

- 2.5D/3D Heterogeneous Integration Technologies for 300 mm wafer:
  - … Package concept development
  - … 3D-SiP/ 3D patterning
  - … FanIn and FanOut WL
  - … RF-FOWLP (AiP)
  - … TSV (via middle, via last, BS-TSV) as well as TGV
  - … W2W stacking/bonding/thinning/TSV/RDL
- 2.5D/3D Interposer:
  - … Si-/glass interposer w/o TSV/TGV, or mixed
  - … HD-RDL (oxide, polymer)
  - … RF-wiring and passives
  - … Sensor & Device integration (active, passives)
- Enhanced high density interconnects and assembly technologies with high accuracy:
  - … Cu/SnAg-µPillar, SnAg-/CuNiAu bumping, Cu-nano wire
  - … Cu-pad for direct bond, Oxide pads for fusion bond, Al-pad formation
- Pre-Assembly & Assembly
  - … Wafer thinning and thin wafer handling technologies with high precision (ultra-thin wafers up to 20 µm)
  - … Wafer mech. & Laser stealth dicing, Laser grooving
  - … D2W, D2D and TC- Bonding, Die stacking
  - … Fine pitch flip chip assembly, mass reflow + underfill
  - … Solder ball and IPD assembly

left:
RDL-1st substrate assembled with SoC

top:
Multi-project wafer for evaluating direct cooling with integrated microchannels



Copper Through Silicon Via (TSV) Formation

Through silicon vias (TSVs) are a key element in 3D wafer-level system integration. Fraunhofer IZM-ASSID has developed a TSV process (POR) for customer-defined applications based on Cu- ECD.

All processes are carried out using advanced, industry-compatible process equipment for 200/300 mm wafers.

Research and development focus:

- High-density Cu-TSV technology (via-last, via-middle, backside via-last) for active circuit devices and interposers
- Application-specific TSV dimensions diameter / depth:
  … min. 5 µm/80 µm
  … typ. 10 µm/150 µm
  … backside TSV (Cu-liner) up to 250 – 700 µm depth
- Cu-TSV filling using high-speed ECD
- Evaluation and qualification of new materials for isolation, barrier/seed and TSV filling
- Optimized via reveal

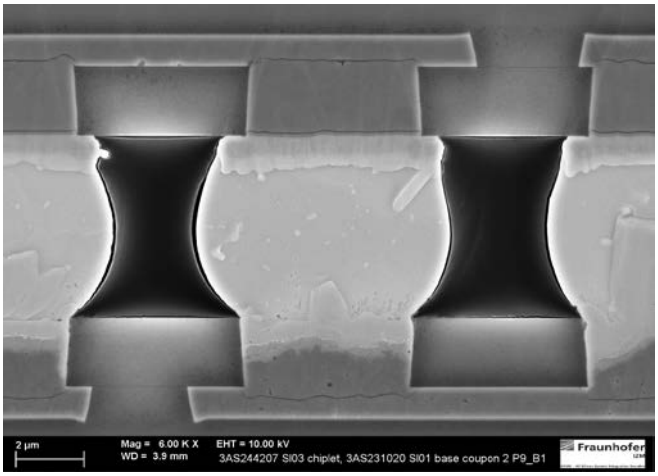
Wafer Thinning and Thin Wafer Handling

Wafer thinning and thin wafer handling technologies are an integral part of the TSV process integration and it is essential for all 3D stacked wafer or die architectures.

Continuous optimization of these technologies is indispensable to meet the requirements of cost-effective manufacturing and the realization of 3D systems.

Research and development focus:

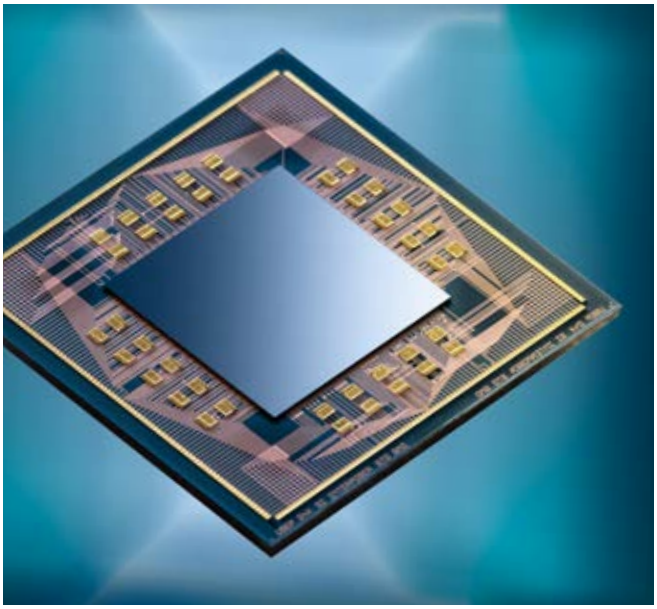
- Optimization of temporary wafer-bonding and de-bonding technologies (device wafer thickness: > 20 µm; multiple repeatable bonding and de-bonding processes)
- Enhanced wafer thinning and stress relief technologies for ultra-thin wafers (> 20 µm, 12")
- Enhanced singulation technologies e.g. stealth dicing for low k-materials, small dicing streets (< 40 µm) and reduced mechanical edge and corner damage to wafer frontside and backside

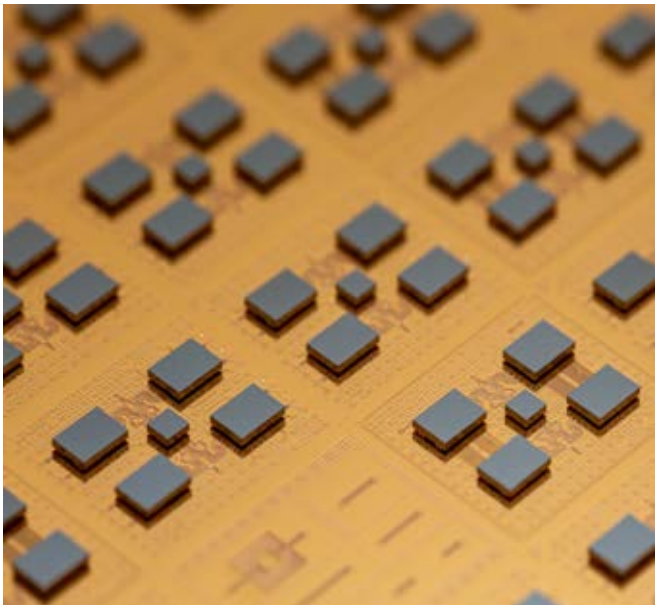


top left:
Cross-section of silicon interposer with 10 x 100 µm Cu-TSV

top right:
Ultra-thinned wafer 300 mm, Wafer thickness: 50 µm

right:
Cross-section: microbump chiplet assembly on Cu/SiO_2 substrate





Interposers with High-Density Redistribution

The TSV interposer is used as a carrier to meet the technical specifications of integrated circuits e. g., geometry, high number of I/O and their high-density routing. The functionality of Si-interposers will be extended by the integration of passive devices such as inductors, resistors and capacitors – with an emphasis on RF applications. Latest generations also include multiple inte- grated active devices e. g. MPU, memories and sensors and deal with high power dissipation by applying innovative cooling architectures and will also address the integration of electrical/optical interconnects for high speed data transmission. Glass interposers with through glass vias (TGV) will be used as a carrier-in-package for RF and SiP approaches. These new generations of interposers are the base line for modularized 3D stacked architectures for fully heterogeneous systems.

Research and development focus:

- Interposers with high-density Cu-TSV
- Glass interposers with TGV
- High-density multi-layer copper wiring: > 2 µm line/space, 4-layer frontside RDL, up to 3-layer backside RDL
- Integration of passive devices (R, L, C)
- Embedding of active and passive devices
- Interposer-based wafer-level packages
- Interposer with integrated microfluidic channels, TSV, electrical and optical interconnects and high-density routing

top left:
Interposer for processor design assessment and functional validation

top right:
RDL-1st substrate Wafer with assembled chiplet

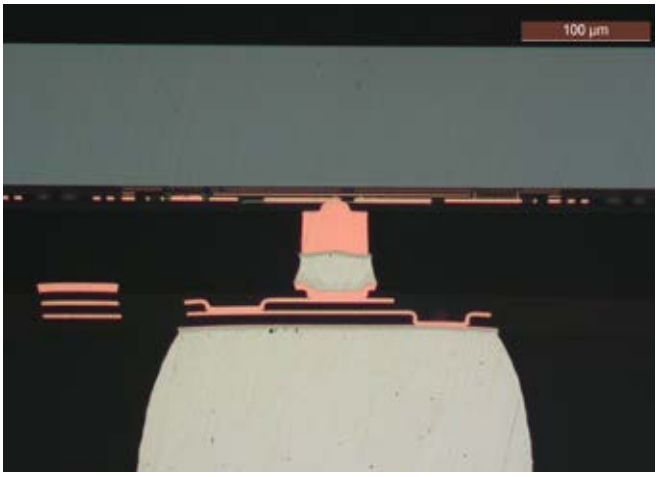
left:
Cross-section of RDL-1st package with chiplet

3D-Assembly and Interconnection Technologies

Assembly and interconnection technologies relevant for 3D system integration are strongly affected by IC technology nodes. Key parameters include die size, number of I/O, pad geometries, passivation layers, wafer-surface topologies, terminal pads and limitations to the thermal budgets that can be applied during assembly. Additional challenges in assembly and interconnect technologies for 3D systems include alignment accuracy, yield requirements and productivity that meet the demands of cost effective manufacturing.

Research and development focus:

- Evaluation of die-to-wafer (D2W), die-to-interposer (D2IP) and wafer-to-wafer (W2W) assembly technologies
- 3D IC assembly with high-density interconnects (> 1000 I/O) and ultra-fine pitch (> 50 µm)
- IC assembly with thin and ultra-thin chips (20 – 150 µm)
- Evaluation of low-temperature assembly technologies
- Evaluation of flux-free solder connections with self-alignment capability



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