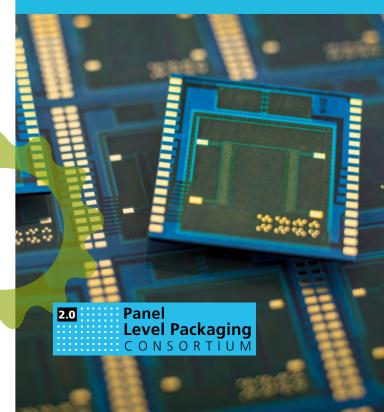




FRAUNHOFER INSTITUTE FOR
RELIABILITY AND MICROINTEGRATION IZM

PANEL LEVEL PACKAGING CONSORTIUM

2019 - 2021 (PLC 2.0)



MEMBERSHIP

Within the Consortium there will be one company membership category. Individual payment plans are available on request. There will be a cancellation clause for the 2nd year. This membership fee covers the fundamental research in all R&D.

Research Results

- Participation in research project steering and controlling
- One-on-one technology transfer

Reports

- Quarterly thrust report
- Half yearly management and technical reports

Meetings

- Quarterly web-meeting
- F2F meeting in Berlin twice a year, including in-depth workshops on specific topics

Further information: https://www.izm.fraunhofer.de/plp

REVIEW OF THE PREVIOUS CONSORTIUM (2016-2019)

Fraunhofer IZM's expertise in wafer level packaging and substrate technology was the nucleus to start the Panel Level Packaging Consortium with 17 industrial partners in 2016. This international Consortium has achieved the overall goals of the project and significant technical progress in the field of large area fan-out panel level packaging.

All partners have contributed to the progress and success of the PLP consortium. Several test layouts were designed for process development on panel sizes of 18"x 24". The implementation and improvement of the die shift compensation as well as the warpage and thickness measurement and evaluation were a joint effort of the different thrusts using over 300,000 test chips. For this metal routing process a fusion of wafer-level (thin film) processing and PCB like substrate processing was developed.

An automated electrical test routine was successfully implemented for the demonstrators. In addition to the technical progress a complex cost modelling has been successfully implemented allowing the cost calculation and analysis with fine granularity of reference applications taking into account process, material and design options, panel utilization and scalability.

CONTACT

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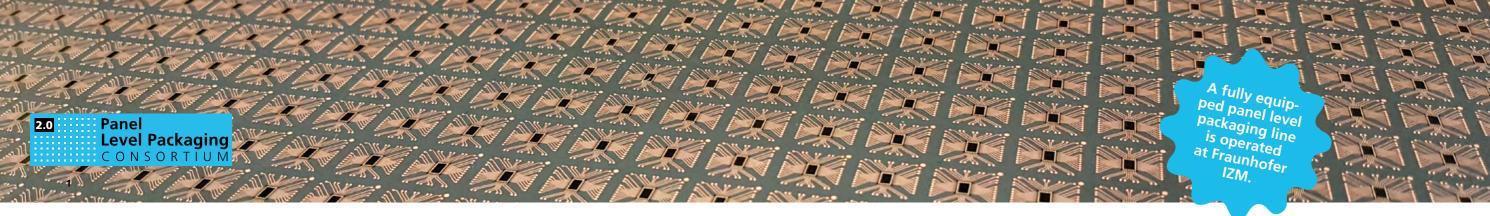
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FOCUS PROJECT FRAME THRUST PROCESS OPTIMIZATION INCLUDUNG COST MODEL

Key benefits

Exploitation is one of the overall technology interactions and limits of FOPLP. In addition, the focus is on the extension of the cost model by a fine line routing model and to other packaging architectures. This will also include a user friendly software modification.

Main goals

- Process considerations along the entire process flow including process and material variations and interactions
- Handling and automatization concepts
- Design and test vehicle preparation
- Study of market and technology developments and networking platform
- Extension of the cost model

FOCUS PROJECT THRUST 1

WARPAGE AND DIE SHIFT

Key benefits

Exploiting die placement and embedding technology for fine line wiring FOPLP.

Main goals

- Process developments for high precision die placement and defined and controlled die shifting
- Evaluation of materials for temporary die attach and embedding
- Investigations of additional parameters on die shift and warpage, such as package density, Si density, ambient conditions, component surface, aspect ratio and others
- Strategies for controlled warpage
- Process flow simulations

FOCUS PROJECT THRUST 2

EXTREME WIRING

Key benefits

Exploiting the technology limits of the fine line wiring.

Main goals

- Realization of 5 µm L/S in up to 3 layers
- Use of adaptive imaging for optimized yield
- Development towards 2 μ m L/S on full IZM panel size (600 x 600 mm²)
- Exploitation of »via-less« Chip-to-RDL interconnection (Suitable structures on chip pad (e.g. small Cu pillar) are used for the penetration through the dielectric film (first RDL layer) during lamination forming an interconnection.)

Additional equipment will be installed by the end of 2019.

FOCUS PROJECT THRUST 3

MIGRATION EFFECTS

Key benefits

Exploiting the migration limits of the fine line wiring.

Main goals

The physical background of these migration phenomena is not new, but larger dimensions are less prone to defects. Therefore miniaturization of the wiring to 2 µm lines/space may face physical/chemical limitations.

Material migration is driven by concentration gradient, temperature gradient, electrical field and mechanical stress Cu is far more resilient to electro-migration compared to Al, but Cu has a much higher tendency to migrate through the dielectric layer further increased by humidity.