Fraunhofer IZM

Wafer-Level System Integration

2.5/3D Integration for High-End Performance Packaging

Fast Facts

1. Custom-specific TSV/TGV integration
2. Organic or inorganic multi-layer routing
3. Chip-to-wafer assembly & encapsulation

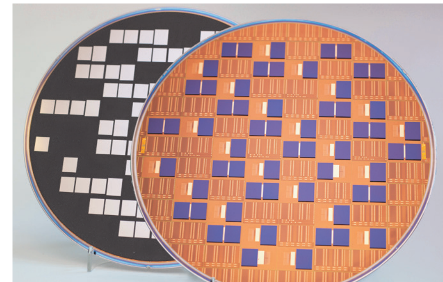
Advanced microelectronic packaging technologies are tremendously important for successful implementation of today's and tomorrow's electronics. The well-established wafer level packaging line for up to 300 mm wafers enables prototyping and small volume production of 2.5D/3D integrated systems, utilizing technologies like wafer-level bumping, wafer level chip size packaging (WL-CSP) and redistribution (RDL), through substrate via or through chip via integration, wafer thinning and handling as well as flip-chip to wafer assembly and encapsulation.

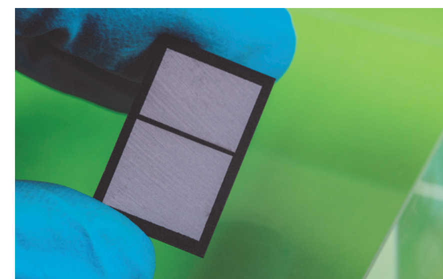
Through-silicon-via (TSV) and through-glass-via (TGV) formation are provided as core technologies for the heterogeneous 2.5D/3D integration of multiple devices such ASICs, processors, memory units, sensors and transceivers with excellent electrical performance in a small form factor to support customized chiplet-based integration and packaging approaches.

The basic technologies for fabricating TSVs in CMOS or bare silicon wafers are dry etching of vias into BEOL and bulk silicon, CVD of insulation layers, and filling of the vias with electroplated copper. Multilayer routing as well as wafer thinning and thin wafer backside processing enabled by temporary wafer bonding are included in regular process flows. TSVs can be formed from the front and the backside of CMOS wafers. In the first case related keep-out zones have to be available for the TSV formation. In the latter case, the TSVs connect to metal pads which are present in the bottom layers of the ICs' front metallization layers (BEOL).

New cost-effective technologies for TGV formation have made glass attractive as a substrate for the 2.5D/3D integration of RF modules and sensor packaging with high wiring density as well. To support related packaging concepts, Fraunhofer IZM has developed TGV metallization processes that generate hermetically filled or liner-coated vias in a low-cost process.

The TSV/TGV technologies are combined with multilayer RDL technologies based on alternated processing of electroplated or sputtered metal tracks and organic or inorganic dielectric layers for insulation. RDLs supporting with low loss/high bandwidth signal transmission for high performance computing (HPC) applications can be achieved by advanced high density copper routing and micro via formation in low-loss polymer dielectrics. The current process allows multilayer RDLs for CSPs or routing on rigid or polymeric flex interposers with up to four layers and with routing densities down to 2 µm line width and 2 µm spacing (4 µm pitch) using polymer vias with 6 µm diameter.





Top: TSV wafer with HD multi-layer routing and ICs before and after molding ((Project STXmod) Bottom: HPC module after wafer molding, balling and singulation

Fraunhofer Institute for Reliability and Microintegration IZM

Kai Zoschke
Phone +49 30 46403-221
kai.zoschke@izm.fraunhofer.de

www.izm.fraunhofer.de