

Chip Assembly Technologies

Chip-to-Wafer Assembly

Fast Facts

1. On up to 300mm wafer size with mult-chip option
2. Placement accuracy from 10µm down to 1µm
3. Flip chip (face down) or die-attach (face up) configuration

Besides wafer-level post processing of semiconductor wafers including TSV integration, redistribution layers and fine-pitch bumping, Fraunhofer IZM has also long term experience in assembly technologies. As part of the department Wafer Level System Integration (WLSI) chip-to-wafer (C2W) assembly technologies offer a broad variety of processes to enable high density microelectronic packaging. One of the major advantages of C2W assembly relies on the fact that it generally offers a higher throughput compared to chip-to-chip assembly.

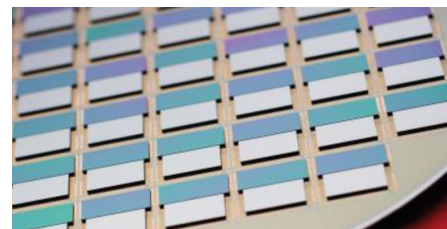
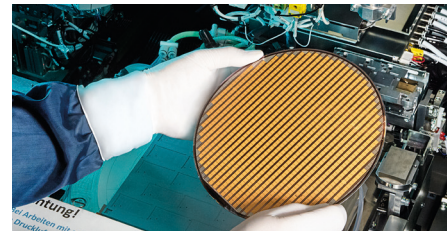
For carrying out wafer level assembly, singulated dies can be directly picked from dicing tape on frame after dicing or from waffle packs. Using mapping files and programming procedures (teaching of chip device and target substrate), known good dies (KGD) or best-in-class dies can be selected and picked from the singulated chip wafer on dicing tape and subsequently assembled at the desired positions of the target wafer. A recognition system allows the matching of the picked-up chip with its final position on the substrate wafer. If

required, the picked dices can also be sorted in waffle packs.

Substrate and chip wafer up to 300 mm size can be assembled with flip-chip bonders of industrial ranks with varying postbonding precision. The most accurate of newest generation achieve a postbond accuracy in the range of 1µm. Substrate wafers can be thin silicon or glass interposer with TSVs on carrier or full thickness active wafers (CMOS). Chip thicknesses down to 50µm can usually be operated on automatic bonders.

Different assembly processes are basically possible using flip-chip or die attach, from thermode bonding, as well as pick-and-place followed by flux-free batch reflow and even up to wafer bonding by means of reconfigured wafer. Here, known good dies are first temporarily bonded on a common temporary carrier wafer (reconfiguration) by means of a temperature resistant adhesive and then simultaneously bonded to their common target wafer substrate.

Thermocompression bonding (Au, In) and soldering (Cu/Sn, SnAg, Au/Sn based) are the most representative interconnecting processes allowing heterogeneous integration. Not only single die but also multiple die can be assembled on a same target substrate, enabling the fabrication of a system-in-package (SiP). All assembly processes are carried out in clean room environment of class ISO 6 (i.e. 1000 FS209) with attention to ESD safety (floor, equipment, persons).



*Top: Pixelated LED dies on CMOS driver wafer
Bottom: 200mm silicon interposer wafer populated with memory and CPU dies*

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