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Fraunhofer Institute for Reliability and Microintegration IZM

Hardware innovations for reliable semiconductor production

Trustworthy electronics through split manufacturing

T4T research project

Demonstrator: 300 mm Si wafer with high-density copper interconnects for chiplet integration as part of the »T4T« project
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The secure supply of electronic components is strategically relevant for Germany as an industrial location. The increasing relocation of integrated circuit (IC) production to regions outside Europe is increasing the risk of malware and espionage functions being inserted into components supplied by contract manufacturers.

In the joint project »Distributed Manufacturing for Novel and Trustworthy Electronics T4T«, several Fraunhofer Institutes and their German industrial partners are developing a split manufacturing approach for semiconductor production. By securely assembling subsystems and encrypting the systems in a trustworthy environment in Germany, the risks of third parties introducing espionage functions or stealing intellectual property in the circuit design (IP) can be substantially minimized.

Target Innovation:

- Integration of the locally produced silicon components directly in packaging on a wafer-to-wafer or die-to-wafer basis (chiplets)
- Development of manufacturing technologies and design processes
- Insertion of a quantum-safe cryptographic key during wafer production

Chip design and processes for split manufacturing

There are currently no standards for the production of highly integrated assemblies with chiplets and W2W processes, nor are there any design rules or assembly design kits (ADKs). Together with Fraunhofer IIS-EAS, Fraunhofer IZM-ASSID is developing process flows for the design phase in distributed manufacturing and checking the design for its technological feasibility.

Advantages of the split manufacturing approach:

- Independent production of individual system components
- Assembly of the complete system, with packaging in Germany
- Protection of the assembled system against illicit copying

Network coordination team

- Robert Bosch GmbH
- Fraunhofer IZM-ASSID

Project partners

- ams-OSRAM International GmbH
- AUDI AG
- DISCO HI-TEC GmbH
- NanoWired GmbH
- X-FAB Dresden GmbH & Co. KG
- X-FAB MEMS GmbH
- Fraunhofer IIS-EAS
- Fraunhofer IPMS
- Leibniz-Institut für innovative Mikroelektronik
- Technische Universität Dresden
- SIJEDA GbR (associated partner)
- SÜSS MicroTec AG (associated p.)

Volume

- € 16.44 million
- 71 % funding share by BMBF

Runtime & Funding reference

- 04/2022 - 03/2025
- BMBF 16ME0481

Roadmap design and demonstrator construction

Working with the project consortium, Fraunhofer IZM-ASSID has developed a roadmap for the »Conceptualization of a work-sharing ecosystem for advanced packaging in microelectronics«.

The institute has also been tasked with producing a technology demonstrator and a working demonstrator for high-end applications with exceptional requirements in terms of performance, reliability, and efficiency.

- Chiplet integration on a Si interposer, pitch 10 µm, combining at least two bonding technologies
- W2W hybrid bond stack consisting of two wafers with encrypted memory

The 300 mm Si interposers have a planar surface on copper and silicon oxide. Three different chiplet sizes (9 x 9 mm, 4 x 4 mm, and 1 x 1 mm) with different connection points are processed as part of the project. Chiplets and interposers have 5 µm small connections on a 10 µm pitch and different bond and test structures.

The plan is to combine hybrid bonds and nanowire chiplets on the hybrid bond surface of a silicon interposer to demonstrate that chiplets from different factories with different surface finishes can be assembled on a single interposer.

The second demonstrator shows the split manufacturing approach in action. Here, the wafers are manufactured in two different »factories« - Fraunhofer IPMS-CNT and Fraunhofer IZM-ASSID - and then assembled in one place using W2W bonding. The project partner SIJEDA is responsible for the cryptographic encryption of the wafer.

Areas of application:

- High-density chiplets for high-performance computing (HPC)
- Chiplets with nanowire bonding for automotive applications
- MEMS inertial sensors for automotive applications
- Encrypted memories for consumer electronics

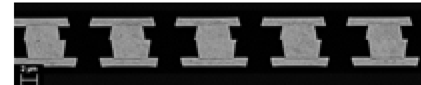
Innovative methods for W2W and D2W bonding with 10 µm pitches

Fraunhofer IZM-ASSID is working on developing stable processes for small hybrid-bonded contacts for the D2W bonding process on 300 mm wafers. The T4T project is working towards a new structuring process by laser direct imaging (LDI) to produce tiny structures at a scale as small as 0.75 µm.

In addition, manufacturing processes for fine in-polymer microbumps and nanowire connections are being refined. The aim is to create 5 µm contacts on a 10 µm pitch - from the initial design to D2W bonding.

- LDI structuring of the copper/oxide redistribution layers and bond sites to match the heterogeneous design
- Development of dry etching processes for oxide structuring
- Copper deposition and chemical mechanical polishing (CMP) for final preparation before hybrid bonding
- Process integration for applying solder to the copper pad and embedding the pad in oxide, followed by subsequent planing
- Process integration for nanowire contact points
- Pre-assembly and assembly for hybrid bonds, microbump, and nanowire chiplets

Hybrid bonding is considered the current enabler technology for the reliable stacking of silicon chiplets with very high contact density (pitch of less than 15 µm, contact diameter of less than 10 µm). This allows the construction of systems with high performance, high data rates, long service lives, and low latency.



Hybrid-bonded interconnects with 10 µm pitch

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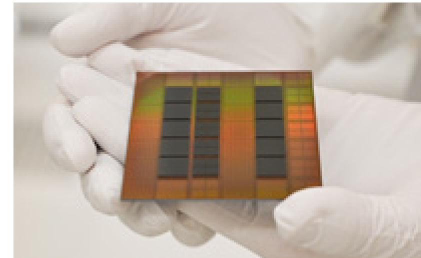

Demonstrator: Assembled chiplets with ultra-fine copper hybrid bond contacts on a pitch of 10 µm

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