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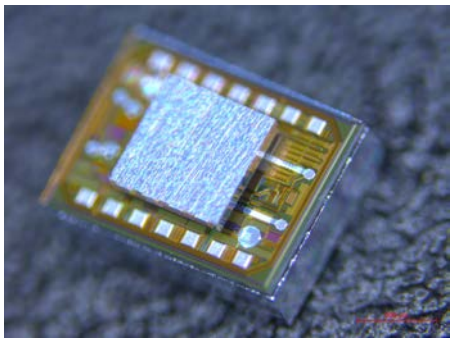
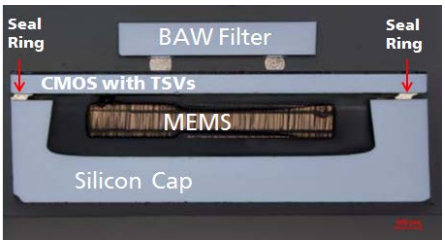
WAFER LEVEL MEMS PACKAGING





Top and cross-sectional view of wafer level packaged timing micro system based on TSV CMOS IC bonded with silicon cap, hermetically sealed quartz crystal and top side mounted BAW filter.

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The combination of active or passive TSV silicon interposer wafers with cap wafers by wafer to wafer bonding technologies offers new possibilities for hermetic wafer level packaging of MEMS components. Based on its 200 mm / 300 mm compatible advanced wafer level packaging process lines, Fraunhofer IZM can support such new hermetic wafer level MEMS packaging concepts. The process scheme includes TSV formation into passive interposer or active CMOS wafers including wafer thinning and thin wafer processing on temporary carrier wafers for TSV back side reveal and RDL / contact formation at wafer back side. Following, the MEMS are assembled onto the back side of the thin TSV wafer which is done by sequential or collective die to wafer bonding. Additionally, cap wafers are manufactured with recesses and metal bond frames to fit exactly to the corresponding TSV wafers with the mounted MEMS. Finally, the cap wafers are bonded to the TSV wafers using a dedicated soldering regime. With that, all mounted components can be hermetically sealed in inert atmosphere or vacuum.

The described approach was evaluted for wafer level packaging of generic timing micro systems. The systems include a special designed timing ASIC build in TSMC 180 nm technology, a miniature quartz tuning fork with 131 kHz resonance frequency as well as a 2 GHz bulk acoustic wave (BAW) filter device.
The ASIC wafers were processed with 100 µm deep Cu TSVs in a front side via last regime. During back side processing of the ASIC wafers proper gold structures for assembly of the quartz components and gold/tin frame structures for bonding of the cap wafers were ceated.
The fabricated cap wafers had a thickness of 400 µm. On these wafers, gold metal frames which match in pitch and lateral dimensions to the frames at the AISC were created. Inside these frames 200 µm deep recesses were etched to generate space for the quartz crystals. Both, ASIC and cap wafers were bonded together in vacuum with standard wafer bonding equipment using a gold/tin soldering regime. After the wafer bonding step, the BAW filter devices were mounted on the ASIC wafer front side using reflow soldering.

The pictures show a top view and a cross sectional view of the created SiPs with a size of 1,64 x 1,25 x 0,65 mm^3. The system delivers real time clock functionalities with one LF and two HF fully programmable output frequencies.

Depending on wafer format, with such a wafer level packaging approach up to several 10k MEMS devices can be hermetically packaged in parallel at one wafer.